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TECHNICAL MANUAL

PHASE JITTER METER

MODEL 45

(HEKIMIAN)

Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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MODEL 45

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SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Model 45 Phase Jitter Meter is designed to measure the phase modulation of "jitter," short-term amplitude variations, and amplitude dropouts resulting from signal transmission through a voice frequency communications channel. High speed data transmission of 1200 bits per second and above are particularly sensitive to these parameters which rank in Importance with signal-to-noise ratio, impulse noise, frequency response, and envelope delay distortion in determining channel error performance. Phase jitter and amplitude variations are introduced by the transmission medium and by terminating, multiplex, carrier, and radio equipment. The ability to measure these important performance parameters and isolate those transmission links or equipment faults which are causing unacceptable performance is an important and necessary function in maintaining a high grade of service.

The Model 45 Phase Jitter Meter measures peak-to-peak and average phase jitter, phase hits, amplitude hits, amplitude dropouts, that exceed 12 dB for a duration of 10 ms or greater, and coincident amplitude/phase hits introduced on a 1.0-kHz carrier transmitted through the voice frequency channel under test. The magnitude of the peak-to-peak and average phase hitter is displayed on a meter, while the remaining measurements are made using individual mechanical totalizers.

The unit is completely self-contained and incorporates a transmit test tone oscillator for making loop measurements without additional equipment. End-to-end measurements can be made using a second Model 45 Phase Jitter Meter or any good quality audio oscillator as a test tone source. A 60-minute timer is incorporated to allow unattended collection of data over preset intervals. When totalized data is not required, flashing indicator lamps are used in place of the mechanical totalizers. An external jitter output is provided to allow chart recording or spectrum analysis. The phase hit, amplitude hit, coincident phase/amplitude hit, and dropout threshold outputs are made available through external outputs on the rack mounting model for use in further defining hit and dropout statistics.

The unit also incorporates a group frequency phase jitter measurement feature which extends the capability of the Model 45 Phase Jitter Meter to group frequency channels. This allows all the parameters normally measured by the Model 45 Phase Jitter Meter in the voice frequency channel to be made at test signal frequencies between 12 and 150 kHz.

The group frequency phase jitter measurement circuit consists of an internal frequency translator which can be operated at as many as five fixed frequencies. At the present time, 18 kHz and 25 kHz are operational; and provisions are made for adding three additional input frequencies between 12 and 108 kHz. A double conversion process is used to minimize all image responses or direct feedthrough when making group frequency measurements.

The Model 45 Phase Jitter Meter is available in rack panel mounting or portable form. The rack mounting form occupies 5-1/4 inches of panel height. All input/output connections are available at rear mounted barrier strips. The input connections for the group frequency measurements are made at the GROUP FREQUENCY INPUT barrier strip located on the

right-hand side of the rear panel. The portable form is self-contained in a hinged cover transit case measuring 8 inches wide, 14 inches long and 9-1/2 inches high.

1.2 SPECIFICATIONS

The mechanical and electrical specifications for the Model 45 Phase Jitter Meter are listed in table 1-1.

Table 1-1. Specifications

INPUT-VOICE FREQUENCY	
Frequency	1 kHz ± 15 Hz
Level	-30 to + 10 dBm
Impedance	600 ohms, 900 ohms (portable only) 10,000 ohms (bridge)
INPUT-GROUP FREQUENCY	
Frequency range	12 to 150 kHz; up to five switch-selected frequencies
Level	-20 to +10 dBm
Impedance	Selected
Input frequency accuracy	± 10 Hz
TRANSMIT OUTPUT	
Frequency	1 kHz ± 2 Hz
Level	-20 to 10 dBm
Impedance	600 ohms
METER	
Peak-to-peak or average jitter	0 to 30 degrees (± 1^{o})
Input/output level	-20 to +2 dBm (± 1.0 dB)
PHASE HITS COUNTER	
Threshold levels (peak)	5 degree steps, 5 to 45 degrees (±1^{o})
Hit resolution	100 ms
Minimum hit duration	4 ms

Table 1-1. Specifications (Cont)

AMPLITUDE HITS COUNTER	
Threshold levels	± 1, 2, 3, and 6 dB
Hit resolution	100 ms
Minimum hit duration	4 ms
DROPOUTS COUNTER	
Threshold level	-12 to -30 dBm (internally adjusted)
Resolution	100 ms
Minimum dropout duration	10 ms
COINCIDENCE COUNTER	
Resolution	100 ms
Minimum coincidence duration	1 ms
EXTERNAL JITTER OUTPUT	
Impedance	20,000 ohms
Level	100 mV/degree (approximately)
EXTERNAL LOGIC OUTPUTS (ALL)	
Impedance	10,000 ohms
Level	Inactive 0.0 V dc Active -10 V dc
TIMER	0-60 minutes
VOLTAGE	105 to 125 V ac, 50-60 Hz
POWER	20 watts
DIMENSIONS	Rack mounting unit, 5-1/4 inches high, 19 inches wide, 15 inches deep Portable unit, 8 inches high, 14 inches wide, 9-1/2 inches deep (with cover)

SECTION II

INSTALLATION

2.1 GENERAL

The Model 45 Phase Jitter Meter is designed for ease of operation and installation. After the unit is removed from its shipping container, perform a complete, external visual inspection for possible damage. To inspect the inside of the rack mounting unit, remove the seven slothead screws retaining the top and bottom covers and perform a visual inspection. To inspect the portable version, remove the two screws along the right- and left-hand edges of the panel; and remove the inner assembly from its transit case. Any damage due to shipping must be immediately reported to the shipping agency.

All internal adjustments are set at the factory, and no further adjustment is required before installation or use of the equipment.

2.2 RACK MOUNTING UNIT INSTALLATION

The unit is mounted in a standard 19-inch relay rack, and requires a standard rack panel height of 5-1/4 inches. Four screws with protective washers are used in mounting the unit.

Primary power is supplied through a line cord packed with the instrument. This cord is connected to a three-pronged ac receptacle located on the rear panel.

Signal input/output lines are connected to either the front panel binding posts or the appropriately marked barrier strips on the rear panel of the instrument. The group frequency measurement input lines are connected to the GROUP FREQUENCY INPUT barrier strip on the right-hand side of the rear panel. Shielded cabling is recommended for all input/output connections.

Connections to the external phase jitter and logic outputs are made to the appropriately marked barrier strip on the rear panel of the instrument.

When these connections are completed, the unit is ready for operation.

2.3 PORTABLE UNIT INSTALLATION

Primary power is supplied through the line cord packed in the compartmented cover of the transit case. The cover is opened by operating the two fasteners holding the compartment lid. The cord is connected to the ac receptacle located through the access hole on the right-hand side of the instrument.

Signal input/output lines are connected to the front panel binding posts or the front panel mounted Western Electric 310 jacks. The group frequency phase jitter measurement signal input is connected to the GROUP FREQUENCY INPUT barrier strip mounted on the front panel of the unit. Shielded cabling is recommended for all input/output connections.

Connection to the jitter output is made using a standard two-circuit, tip-sleeve phone plug. The phase hit, amplitude hit, coincident, and dropout logic outputs are not available externally on the portable unit.

For fixed station applications, a rack mounting shelf is used. This shelf mounts in a standard 19-inch relay rack and occupies 10-1/2 inches of vertical rack space. The behind-the-panel depth is 12 inches, which includes storage provisions for the transit case cover.

SECTION III

OPERATION

3.1 GENERAL

This section contains a description of the controls, indicators, and connectors, and operating procedures for the Model 45 Phase Jitter Meter. Before operation, ensure that all connections to the instrument are made in accordance with the instructions in section II, Installation.

3.2 CONTROLS, INDICATORS, AND CONNECTORS

The controls, indicators and connectors used in operating the Model 45 Phase Jitter Meter are described in table 3-1. All controls and indicators are located on the front panel. No internal adjustments are required during normal operation. Adjustment procedures for internal controls are contained in section V, Maintenance.

Table 3-1. Phase Jitter Meter Control, Indicator, and Connector Descriptions

NAME	REFERENCE DESIGNATION	FUNCTION	FIGURE
POWER pushbutton indicator	S203 DS206	Applies power to unit. Lights to indicate power is applied	5-2
INPUT terminals	TB201, J205, 206, 207	Provides input connections for voice frequency signal. Connections for wire leads, clip leads, banana plugs, and Western Electric 310 plugs.	5-2
GROUP FREQUENCY INPUT terminals	TB601	Provides input connections for group frequency signals.	5-2
INPUT switch	S201	Selects input line terminations of 600 ohms, 900 ohms (portable unit only), or bridging (10,000 ohms).	5-2
INPUT selector switch	S601	Selects voice frequency operation or up to five group test frequencies: VF, 1, 2, 3, 4, 5.	5-2
METER switch	S204	Selects input to the front panel meter. Measures input/output level, peak-to-peak jitter, average jitter, reference set level, and relative frequency of the phase-locked oscillator.	5-2

Table 3-1. Phase Jitter Meter Control, Indicator, and Connector Descriptions (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION	REF. FIGURE
		Switch Positions LEVEL SET INPUT LEVEL OUTPUT LEVEL FREQ SET AV JITTER P-P JITTER	
FREQ control	R202	Adjusts frequency of the phase-locked oscillator to coincide with input frequency	5-2
METER	M201	Displays parameter selected by the meter switch.	5-2
LEVEL SET control	R223	Sets input signal at an internal reference level of 0 dBm.	5-2
PEAK DEGREES switch	S205	Selects the threshold to degrees (peak) which must be exceeded by the phase jitter to be totalized on the PHASE HIT counter.	5-2
PHASE HITS counter	L203	Totalizes the number of phase impluses exceeding the threshold setting.	5-2
PHASE HITS indicator lamp	DS204	Flashes when a phase hit is detected when S207 is in the FLASH position.	5-2
+DB AMPLITUDE HITS switch	S206	Selects the threshold in dB which amplitude fluctuations must exceed before being totalized on the AMPLITUDE HITS counter.	5-2
AMPLITUDE HITS counter	L204	Totalizes the number of amplitude hits exceeding the level set on S206.	5-2
AMPLITUDE HITS Indicator lamp	DS203	Flashes when an amplitude hit is detected when S207 is in the FLASH position.	5-2
COINCIDENCE counter	L205	Totalizes the number of coincident phase/amplitude hits which exceed their respective thresholds. Counts multiple hits from one source during an extended duration hit from the other source.	5-2
COINCIDENCE indicator lamp	DS202	Flashes when coincident phase/amplitude hits are detected when S207 is in the FLASH position.	5-2

Table 3-1. Phase Jitter Meter Control, Indicator, and Connector Descriptions (Cont)

NAME	REFERENCE DESIGNATION	FUNCTION	REF. FIGURE
DROPOUTS (-12 DB/ 10 MS) counter	L206	Totalizes the number of dropouts which fall below the internally set level (typically -12 dBm) for longer than 10 milliseconds. When a dropout has occurred, all other counters/indicators are inactivated.	5-2
DROPOUTS (-12 DB/ 10 MS) indicator lamp	DS201	Flashes when a dropout has occured and S207 is in the FLASH position.	5-2
TIMER switch	S202	Automatic timer to allow unattended accummulation of data for known time intervals. Continuous operation provided in HOLD position.	5-2
TIMER indicator light	DS205	Glows when the timer is in the ON position.	5-2
COUNT-FLASH switch	S207	Selects operation of either the counters or indicator lamps.	5-2
OUTPUT terminals	TB202, J208, 209, 210	Provides connection to the transmit oscillator, for wire leads, clip leads, banana plugs, and Western Electric 310 plugs.	5-2
OUTPUT LEVEL control	R215	Controls level of the transmit oscillator output.	5-2

3.3 OPERATING PROCEDURES

3.3.1 INPUT/OUTPUT LEVEL

To ensure proper operation of the instrument, the input and output (if used) levels are checked prior to a measurement. This is performed by selecting the appropriate position of the meter switch. The meter indicates in dBm for all input terminations. For inputs below -20 dBm (the instrument operates down to -30 dBm input levels), a separate, more sensitive level meter must be used. The output level is adjusted using the OUTPUT LEVEL control.

3.3.2 LEVEL MEASUREMENT (GROUP FREQUENCY)

All adjustments and measurements are made in an idle group frequency channel using a test signal. The test signal frequency must be within ±10 Hz of the specified test frequency. Measurements are normally made at a -10 dBm level; however, signal levels -20 and +5 dBm can also be used.

When making measurements, the test signal generator must be checked to ensure that it provides a jitter-free output. This is performed by connecting a local Model 45 Phase Jitter Meter directly across the generator's output. Commercial generators typically have less than 1 degree peak-to-peak jitter for test frequencies below 10.0 kHz. However, at higher test frequencies the generator could contribute more jitter than the channel under measurement. Periodic verifications of the test signal generator phase jitter performance must be made using the Model 45 Phase Jitter Meter.

The group frequency level measurement allows direct test signal input level measurements on the INPUT LEVEL position of the Model 45 Phase Jitter Meter. These level measurements are made with respect to 1 milliwatt across the selected input impedance (dBm).

After the above conditions are satisfied, set the INPUT selector switch to the desired group test frequency positon (5 maximum). All other controls are adjusted in accordance with the following operating procedures.

3.3.3 LEVEL SET ADJUSTMENT

After determining that the proper input signal level is present, the level set adjustment is made. Set the meter switch to the LEVEL SET position and adjust the LEVEL SET control for a meter indication of 0 dBm. This adjusts the instrument's internal reference level for optimum operation of the phase jitter and amplitude sensitive circuitry.

If long-term input level changes during the test exceed ±3 dB, readjust the LEVEL SET control.

3.3.4 FREQUENCY ADJUSTMENT

After proper input/output levels are established, the internal reference phase-locked oscillator is "locked" to the incoming carrier frequency. This is accomplished by setting the meter switch to the FREQ SET position and adjusting the FREQ control for a meter indication at the FREQ SET mark (half scale). Proper operation is verified by rotating the FREQ control over its entire range and noting a corresponding deflection of the meter over approximately 80 percent of its scale. It is possible for the reference oscillator to lose lock at the extreme settings of the FREQ control. This is indicated by an oscillation of the meter needle, which decreases in frequency as the locked oscillator condition is approached. When phase-lock is obtained, the oscillation stops and the meter indicates near one end of its scale. As rotation of the FREQ control is continued, the meter deflects toward the FREQ SET mark. When this is verified, set the meter to the FREQ SET mark. This occurs near the midrange of the FREQ control. Valid measurements can now be made.

If the input frequency is offset from the nominal 1.0 kHz, but remains within the range of the instrument, rotate the FREQ control from its midrange position to set the meter on the FREQ SET mark. If the FREQ SET mark cannot be set, the test signal frequency error is excessive; and the transmit frequency must be checked and adjusted.

When the test tone frequency is outside the range of the instrument, the FREQ control has little or no effect on the meter indication. The meter remains near the FREQ SET mark regardless of the FREQ control position. When this indication is obtained, independent measurements must be made to verify the test signal frequency.

3.3.5 AVERAGE PHASE JITTER

The average phase jitter is measured by setting the METER switch to the AV JITTER position and reading the value on the meter scale. A maximum value of 30 degrees can be measured.

3.3.6 PEAK-TO-PEAK PHASE JITTER

Peak-to-peak phase jitter is measured by setting the METER switch to the P-P JITTER position. Peak-to-peak phase jitter values up to 30 degrees can be measured.

3.3.7 PHASE HITS MEASUREMENT

The phase jitter occasionally shows large, rapid variations in phase. These phase impulses, or "hits," are totalized using the phase hits counter. The counter operation is controlled by means of the TIMER and COUNT-FLASH switches.

The phase threshold, which a hit must exceed before it is totalized, is set by means of the PEAK DEGREES selector switch. As an example, when the switch is set to 25 degrees, any positive or negative phase hit which exceeds 25 degrees for more than 4.0 milliseconds results in an additional count being added to the total displayed on the counter. Phase hit peak degree threshold levels from 5 to 45 degrees in 5-degree steps are provided by means of the PEAK DEGREES selector switch. The counter is reset to zero using the small toggle lever located on its front bezel.

Note

The counter measures peak phase hits as differentiated from the peak-to-peak jitter measured by the meter.

3.3.8 AMPLITUDE HITS MEASUREMENT

The test tone frequently shows rapid variations in amplitude. These variations or hits are totalized using the amplitude hits counter. The counter operation is controlled by means of the TIMER and COUNT-FLASH switches.

The amplitude threshold, which a variation must exceed before it is totalized, is set by means of the ±DB AMPLITUDE HITS selector switch. As an example, when the switch is set to ±3 DB, any amplitude variation either plus or minus which exceeds this level for more than 4.0 milliseconds results in an additional count being added to the total displayed on the counter. Threshold levels of ± 1, 2, 3, and 6 DB are provided. The counter is reset to zero using the small toggle lever located on its front bezel.

3.3.9 COINCIDENT PHASE/AMPLITUDE HITS MEASUREMENT

To provide insight into the mechanism causing the phase and amplitude hits, a coincidence counter is provided which totalizes simultaneous phase and amplitude hit occurrences. No controls are associated with the COINCIDENCE indicator, and its operation is controlled by means of the TIMER and COUNT-FLASH switches.

The coincidence counter totalizes multiple hits from one source when an extended duration hit is occurring on another source. If, during a long duration amplitude hit, several phase hits occur, the individual phase hits are totalized on the coincidence counter. Thus, the coincidence counter indicates a number of coincident hits which exceeds either value shown on the phase and amplitude hits counters.

The counter is reset to zero using the small toggle lever located on its front bezel. When the COUNT-FLASH switch is in the FLASH position, the counter is disabled; and coincidence hits are indicated by a flashing of the coincidence indicator lamp.

3.3.10 DROPOUT MEASUREMENT

The number of amplitude dropouts on the circuit is measured by the dropouts counter. The dropout threshold level is internally set between 12 and 30 dB. After a dropout occurs, the amplitude hits, phase hits, and coincidence counters are disabled until the input signal again exceeds the dropout threshold.

For accurate dropout detection, the LEVEL SET control is adjusted to provide a 0-dBm indication on the meter in the LEVEL SET position with the nominal test tone level applied.

To be detected as a dropout, the amplitude variation must exceed the dropout threshold for a period exceeding 10 milliseconds. Amplitude variations of less than this duration or amplitude are not counted as dropouts.

The dropout threshold is set internally as described in section V, Maintenance. This is set at the factory at -12 dB in accordance with established Bell System practices.

The counter is reset to zero using the small toggle lever located on its front bezel. When the COUNT-FLASH switch is in the FLASH position, the counter is disabled; and dropouts are indicated by a flashing of the DROPOUTS (-12 DB/10 MS) indicator lamp.

3.3.11 TIMER OPERATION

Operation of the counters and indicator lights is controlled by means of the timer. For timed measurements, the timer is set to the desired number of minutes. At the end of this time period, the timer is at zero and counter operation is inhibited. For continuous operation, the timer control is rotated clockwise to the HOLD position.

Note

When recorded data is not to be gathered, set the COUNT-FLASH switch to the FLASH position. This reduces the mechanical wear in the counting units.

When the timer is in the ON condition, the COUNT-FLASH switch is used to select either the counters for totalized information or the flashing indicator lights.

Note

The timer control must be rotated past 10 minutes to fully activate its spring mechanism. For durations less than 10 minutes, the timer control is then returned to the desired interval. If this is not done, time intervals of less than 10 minutes are not accurately timed.

3.3.12 EXTERNAL PHASE JITTER OUTPUT

The external phase jitter output makes available for external chart recording or spectral analysis the jitter output of the phase detector. Its output impedance is approximately 20,000 ohms, and it must be connected only to high input impedance devices. The open circuit voltage at this point is approximately 100 millivolts/degree of phase jitter. The jitter energy lies between 10 and 250 Hz as determined by the internal low-pass and high-pass filters incorporated in the instrument.

3.3.13 EXTERNAL THRESHOLD LOGIC OUTPUTS

Logic outputs for the threshold detectors associated with the phase hits, amplitude hits, phase/amplitude coincident hits, and dropouts are provided on a rear mounted barrier strip, in the rack mounted version. When a threshold is exceeded, the logic level drops to a -10 volts dc. The duration of the pulse is equal to the time the threshold level is exceeded.

These outputs are not made available on the portable unit.

SECTION IV

THEORY OF OPERATION

4.1 GENERAL

The Model 45 Phase Jitter Meter is entirely solid-state and makes extensive use of integrated circuit differential operational amplifiers as well as conventional discrete components. The design makes use of modern design techniques in both the analog and digital circuitry.

A simplified block diagram of the Model 45 Phase Jitter Meter is shown in figure 4-1. The signals to be tested are either voice frequency channel test tone signals or group frequency channel test signals at 18 kHz, 25 kHz, or any one of three other frequencies between 12 kHz and 108 kHz. To test voice frequencies, set the INPUT termination switch to BRIDGE or 600 OHM, as necessary, and set the INPUT selector switch to VF (voice frequency) to bypass the frequency translator. Then, the incoming test tone signal is first terminated in the desired impedance before reaching the input amplifier. The LEVEL SET control is used to set the gain of the input amplifier to provide a fixed reference level at its output. This signal is then fed to the two major functional blocks of circuitry, one associated with the phase jitter measurement and the other with the amplitude, coincidence, and dropout measurements.

To test group frequencies, set the INPUT selector switch to the desired group frequency position. Then, the input test signal is transformer-coupled to the first crystal controlled frequency translator. This translator heterodynes the input frequency up to the 455-kHz IF filter. Up to five different crystal frequencies are switch-selected for this translator. The filtered IF signal is heterodyned down to 1.0 kHz by the second crystal controlled, fixed frequency translator. This translator is followed by a multisection, low-pass filter, to eliminate the translation carrier, and an emitter-follower audio amplifier used to isolate the output signal. The 1.0-kHz output signal is connected through the INPUT selector switch to the input amplifier.

The signal from the input amplifier is connected to the input limiter of the phase jitter detector circuitry. The output of the limiter is a square wave replica of the input signal zero crossings, and becomes one input to the digital phase detector. The phase detector compares this signal to the phase-locked reference oscillator and generates dc pulses whose widths are proportional to the phase difference. These pulses are then changed to a dc voltage proportional to the phase difference by the 300-Hz low-pass filter. This output is used to control the phase-locked reference oscillator, which has a loop bandwidth of approximately 5 Hz. The filtered phase detector output is also applied to an ac coupled amplifier which removes the dc component from the phase detector output. This jitter signal is then full-wave rectified and applied to the average and peak-to-peak metering circuit.

The phase impulse counter uses an adjustable threshold detector to detect phase excursions above a preset threshold. Each time a positive or negative phase excursion exceeds this threshold, a pulse is generated which drives the phase hits counter or indicator lamp.

The signal applied to the amplitude measurement circuitry is processed by a wide dynamic range automatic level control (ALC) circuit incorporating a voltage controlled attenuator, full wave rectifier, and peak detector. The output level of this circuit remains constant

within ±2 dB for input range variations of 30 dB. Level corrections are made with a time constant of approximately 10 seconds. The output of the full wave detector is filtered in a 250-Hz low-pass filter and applied to the reference amplifier and the high/low gain hits comparator. This circuit detects amplitude variations exceeding the preset threshold values and generates a pulse signal which drives the amplitude hits counter or lamp.

Before reaching the automatic level control (ALC), the signal is monitored by the dropout detector and dropout comparator. When the absolute signal level drops 12 dB or greater below the comparator threshold level, a pulse is generated which activates the dropout counter or lamp. A dropout must exist 10 milliseconds before recognition is made. During a dropout period, all the other counters and lamps are disabled until the signal level rises above the dropout threshold.

The outputs of the phase and amplitude hit comparators are combined in an AND gate to generate the driving pulse for the amplitude/phase coincidence counter. When both hits are simultaneously present for 1 millisecond or longer, a coincidence hit pulse is generated and fed to the counter or indicator light.

The stable 1.0-kHz transmit test tone oscillator incorporates a line amplifier which is transformer-coupled to the balanced transmit output.

The meter switch allows the meter to monitor the input or output test tone levels, the set level reference value, the outputs of the peak-to-peak or average jitter detectors, and the control loop of the phase-locked reference oscillator.

Power for the instrument is supplied by an electronically regulated, dual power supply providing +15 and -15 volts dc, from which all operating voltages are derived.

A 60-minute timer, with a HOLD position, controls the power to the counters and allows unattended measurements to be performed.

The following paragraphs describe in detail the circuit operation of the Model 45 Phase Jitter Meter.

4.2 DETAILED CIRCUIT OPERATION

4.2.1 INPUT

The voice frequency and group frequency input signals are connected using the three-way binding posts, the Western Electric 310 jack (portable unit only), or the rear mounted barrier strips (rack mounting unit only). Both balanced and unbalanced signals are accommodated. The voice frequency input is terminated by INPUT switch S201. The group frequency input is terminated at the frequency translator input (T601).

4.2.2 SIGNAL SWITCHING

The operation of the frequency translator is controlled by INPUT selector switch S601. During normal VF (voice frequency) operation, the 1-kHz input terminals are connected directly to the amplitude jitter detector input circuitry via the INPUT selector switch. When a group frequency is selected, the INPUT selector switch applies +15 volts to the frequency translator and connects the translator's audio output to the amplitude jitter detector input. The INPUT selector switch also connects the proper crystal/trimmer circuit to match the desired input frequency.

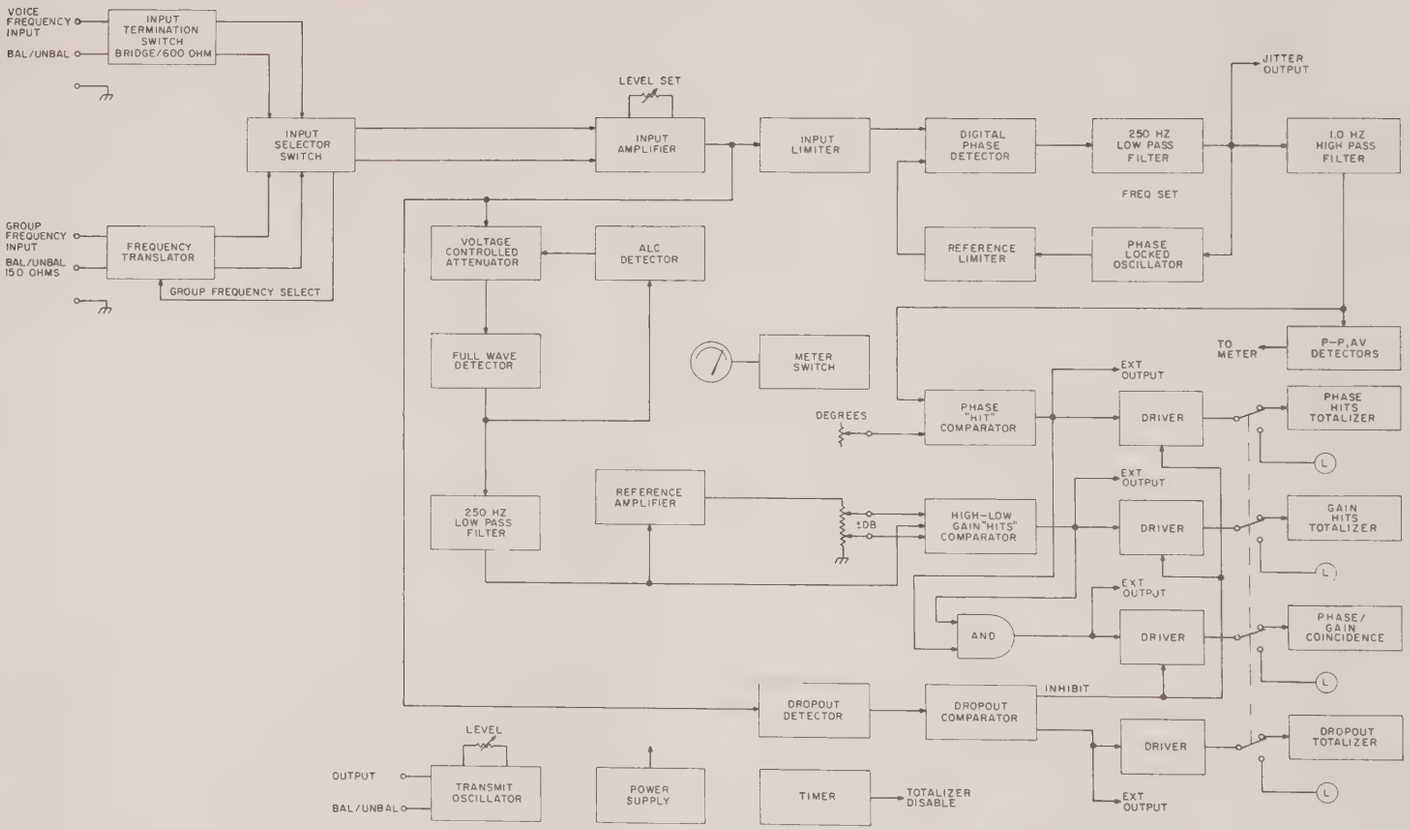


Figure 4-1. Phase Jitter Meter, Block Diagram

The +15 volt power for the frequency translator is obtained directly from the Model 45 Phase Jitter Meter's power supply.

4.2.3 FREQUENCY TRANSLATOR

The input signal from the GROUP FREQUENCY INPUT connector TB601, is connected to input matching transformer T601 through attenuator network R601, 602, 603. The attenuator network sets the overall gain of the first crystal controlled frequency translator, IC601, and provides impedance matching for the input signal. The input transformer is connected for either balanced or unbalanced operation, and is a wideband unit designed for operation from 10 kHz to 1 MHz. The transformer is terminated by resistor R604.

The input signal is then applied to the first crystal controlled translator, IC601, which contains an oscillator/balanced-mixer circuit. The oscillator circuit is crystal controlled using crystals CR601 through 605. Individual frequency adjustments are provided by trimmer capacitors C601 through 605 and padding capacitors C607 through 611. The oscillator signal, along with the input signal, is injected into the balanced mixer whose output is connected to the 455-kHz IF filter, F601. The filter uses ceramic elements, and has a bandwidth of 4.0 kHz. It rejects undesired signals in the group channel and removes the heterodyning carrier from the frequency translator output.

The filtered signal from the 455-kHz IF filter, F601, is applied to the second crystal controlled fixed frequency translator, IC602, operating at a fixed crystal frequency of 454.0 kHz. This translates the IF signal down to the 1.0-kHz test frequency used by the Model 45 Phase Jitter Meter. The oscillator frequency is adjusted by trimmer capacitor C606.

The translator output is filtered by the two-section RC filter consisting of R609, 610 and C619, 621. The output gain is controlled by variable resistor R613 which feeds emitter-follower audio amplifier Q601. The output of this amplifier then feeds input amplifier (IC401A) of the amplitude jitter detector when INPUT selector switch S601 is in the group frequency position.

DC line currents are blocked by input coupling capacitors C401, 402; and transient voltage protection is provided by diodes D401 through 404. Differential operational amplifier IC401A provides conversion of the unbalanced input signal to a balanced output signal with a gain controlled by LEVEL SET control R223. Amplifier phase compensation is provided by R405 and C403, 404. The LEVEL SET control is adjusted to provide a 0-dBm meter indication, with the meter switch in the LEVEL SET position. The output of this amplifier is used to feed both the phase jitter and amplitude detection circuitry.

The input level meter is connected through a separate dc blocking capacitor, C135, to minimize phase shift introduced by the switching of the meter load across capacitors C401, 402.

4.2.4 PHASE JITTER INPUT CIRCUITRY

Differential operational amplifier IC-101A operates as an open loop gain zero crossing detector with dc stabilization provided by R103, 104 and C104. Amplifier phase compensation is provided by R106 and C108.

4.2.5 DIGITAL PHASE DETECTOR

The output from IC-101A and the phase-locked reference oscillator output from IC-101B are connected to the two inputs of the digital phase detector. Transistors Q101 and Q102 and associated components form an exclusive-OR gate which provides a bipolar output pulse whose width is proportional to the phase difference (zero crossings times) of the two inputs.

Back-to-back zener diodes D107, 108 provide a constant amplitude pulse to the following circuitry.

4.2.6 LOW-PASS FILTER

The carrier frequency present at the output of the digital phase detector is removed and the upper limit of the phase jitter spectra determined by the low-pass filter consisting of IC-102B and its related components. This filter provides a three-pole butterworth response using active filter design techniques. The filter elements consist of R113, 114, 115, 117 and C105, 106, 110. Components R116 and C103, 107 are phase compensating networks for the operational amplifier.

4.2.7 PHASE LOCKED REFERENCE OSCILLATOR

The output of the low-pass filter is a dc voltage proportional to the instantaneous phase difference between the input and reference signals. This voltage is filtered by the network consisting of R162, 163, and C124 to provide an overdamped phase-lock loop response characteristic. The filtered voltage controls a conduction angle reactance modulator consisting of emitter follower Q104 and C125, D119. This circuit effectively varies the capacitance across the oscillator tank circuit consisting of L101 and C129, 128. The oscillator frequency is varied by means of the front panel FREQ control and its associated capacitor, C126. The oscillator output is connected to the input of the reference limiter, IC-101B, which furnishes the limited reference signal to the digital phase detector.

The average dc value of the digital phase detector output is zero when the phases of the input and reference signals are properly related. This is monitored by the meter using multiplier resistor R118 and bias resistors R119, 120.

4.2.8 AC COUPLED AMPLIFIER AND FILTER

The output of the low-pass filter is connected to an ac coupled amplifier and filter consisting of IC-102A and its related components. C140 provides an additional filter section; and R123 and C112, 113 provide phase compensation for the operational amplifier. The output of IC-102A is applied through isolation resistor R126 to the external jitter output.

4.2.9 AVERAGE DETECTOR

The average value of the phase jitter is measured by performing a full-wave rectification of the phase jitter signal and applying this to the metering circuit. The full-wave detector consists of IC-103A, 104B. IC-103A is used as a half-wave rectifier with feedback to eliminate the effects of the diode rectifier offset voltages. The negative half-wave rectified signal is summed through R132 and 131 with the original input signal, and the resulting full-wave rectified waveform is amplified by IC-104B. This circuit provides a highly stable, precision, full-wave rectifier, independent of diode offset characteristics. Its output is applied to the meter through R138 and calibration resistor R139. The meter displays the average value of the rectified phase jitter signal.

4.2.10 PEAK-TO-PEAK DETECTOR

Peak-to-peak detector IC-103B utilizes the output of IC-103A to provide a signal compensated for diode offset voltages in both the positive and negative direction. IC-103B is a unity gain driver amplifier for positive peak detector D111, R143, C120 and negative peak detector D112, R144, C121. The outputs of these peak detectors are applied to the meter through

resistor R146 and calibration resistor R145. The detector time constant provides peak detection of repetitive signals down to the low frequency cutoff of the phase jitter signal.

4.2.11 PHASE HITS DETECTOR

The full-wave rectified jitter signal is applied to differential amplifier threshold detector IC-104A, which compares this signal to the threshold level set by PEAK DEGREES switch S205. The output of the amplifier remains at a positive value until the phase jitter signal exceeds the threshold level. When this occurs, the output abruptly changes to a negative voltage; and when the input falls back across the threshold voltage, the output returns to the positive level.

The hit transition is processed by a 4-millisecond "time out" circuit consisting of Q502 and IC-501A located on PC board HLI TO-1. A positive voltage at the base of Q502 clamps the RC time-constant circuit, R508, C502, to ground, and results in a positive voltage output from trigger amplifier IC-501A. When a phase hit occurs, Q502 is opened allowing C502 to charge toward the supply voltage. The time constants are arranged so the capacitor voltage crosses the trigger amplifier threshold in 4 milliseconds, resulting in a change of state of the trigger amplifier output. This change is used to drive the phase hits multivibrator and logic output. If the phase hit is ended before the 4-millisecond interval, the capacitor is immediately clamped to ground, terminating its charging cycle. Thus, phase hits of less than 4-millisecond duration will not trigger the phase hits multivibrator.

4.2.12 AUTOMATIC LEVEL CONTROL CIRCUITRY

The automatic level control circuitry consists of amplifier and full wave rectifier IC401B, 402A; peak detector D409; and FET voltage controlled attenuator Q421, R406. These circuits provide output variations of less than ±2 dB for a 30-dB range of input levels.

The input signal is applied to R406 which forms a voltage divider with the voltage controlled resistance of FET transistor Q421. This attenuated voltage is then applied to full wave rectifier IC401B, which incorporates a bridge rectifier, D405 through 408, in its feedback loop. Amplifier dc stabilization is provided by R413 and C408, and phase compensation by R407 and C406, 407. This circuit arrangement automatically compensates for the diode offset voltages. The positive and negative waveforms are summed and inverted in unity gain amplifier IC402A, which provides at its output a full-wave rectified replica of the input signal at IC401B. The full-wave rectified signal is applied to peak detector D409, C411, which develops the dc control voltage for the voltage controlled attenuator, transistor Q421. A dc offset control, R418, is provided for setting the operating point of Q421. Its adjustment is covered in section V, Maintenance. The 10-second time constant of the ALC loop is provided by R416 and C405.

4.2.13 LOW-PASS FILTER

The carrier frequency present at the output of the full-wave detector is removed and the upper limit of the amplitude variation is determined by the low-pass filter consisting of IC402B and its related components. This filter provides a 250-Hz, three-pole butterworth response using active filter design techniques. The filter elements consist of R419 through 422, and C412, 413, 414. Components R423 and C416, 415 are phase compensating networks for the operational amplifier.

4.2.14 AMPLITUDE HITS DETECTOR

The amplitude hits detector consists of dual threshold detectors IC404A, 404B, set to activate whenever an increase or decrease in signal level occurs which exceeds the ±DB switch setting. The outputs of these detectors are then combined and used to drive the "time out" circuit followed by the amplitude hits counter or indicator lamp.

Amplitude threshold detectors IC404A, 404B compare the output of the low-pass filter containing the short-term amplitude variations with a long-time constant reference voltage generated by reference amplifier IC403A. Decision hysteresis is provided in the threshold detectors by resistors R428, 429, and R430, 431, respectively. Phase compensation is provided by C421, 422 and C423, 424, respectively.

Reference amplifier IC403A obtains the long-term average of the low-pass filter output through R424 and C420. This is then applied to the input of amplifier IC403A and amplified by a factor of 2. The gain is controlled by the resistor divider network consisting of R425, 426 and 216 through 222. The ±DB switch, S206, selects the voltages on this divider chain corresponding to ±1, 2, 3, or 6 dB levels. These voltages then form the reference inputs to amplitude threshold detectors IC404A, 404B.

The outputs of threshold detectors IC404A, 404B are combined by diodes D410, 411, and applied to the 4-millisecond "time out" circuit consisting of Q501 and IC501B located on PC board HLI TO-1. Its operation is identical to the phase hits "time out" circuit discussed in paragraph 4.2.11, except a hit is indicated by a positive rather than a negative voltage. The "time out" circuit output is connected to transistors Q401, 402, which furnish the driving signals to the one-shot multivibrators driving the amplitude hit and coincident hit indicators, respectively.

The external logic outputs are obtained from the collectors of these driver transistors through isolating resistors R469, R450.

4.2.15 DROPOUT DETECTOR

The dropout detector measures dropouts that exceed 12 dB for a duration of 10 milliseconds or greater. The dropout detector is activated when the input signal exceeds 12 dB below the input reference level established by means of the LEVEL SET control. This circuit is contained on printed circuit board HLI 45-400A, which is mounted and secured to amplitude detector board HLI 45-3 and receives its operating power from the instrument's regulated power supply.

The dropout detector consists of an amplitude detector, low-pass filter, threshold detector, and timing circuit. Input amplifier IC401A and LEVEL SET control R223 are used to provide a 0-dBm reference level at terminal W of HLI 45-3. This reference level signal is also connected to terminal D of dropout detector board HLI 45-400A.

The input signal is applied to the full-wave amplitude detector consisting of IC1A and IC2A. This circuit provides a highly stable precision full-wave rectifier independent of diode offset characteristics. Its output at IC2A, pin 1, represents the peak value of the input signal.

The full-wave amplitude detector consisting of IC1A and IC2A is followed by a five-pole, active, 300-Hz low-pass filter consisting of IC3A and IC3B. The filter removes the carrier frequency components present at the output of amplitude detector IC1A, IC2A and provides an overall gain of 6 dB.

The dropout detector monitors the input signal level from the 300-Hz, low-pass filter IC3A and IC3B, and is activated when the input signal drops 12 dB below the reference level for a period exceeding 10 milliseconds. The reference level is set when LEVEL SET control R223 is adjusted for a 0-dBm meter indication in the LEVEL SET meter position.

The dropout detector consists of threshold detector IC2B and timing circuit Q1 and IC1B. The low-pass filter, IC3A and IC3B, output is connected to one input of threshold detector IC2B where it is compared against the threshold voltage set by R17. This is factory set at -12 dB.

The timing circuit consists of Q1 and IC1B. When a dropout occurs, Q1 is turned off, allowing C6 to charge toward the supply voltage. This time constant is selected so that the capacitor voltage crosses the trigger amplifier threshold in 10 milliseconds, resulting in a change of state of the trigger amplifier output. This change is used to drive the dropout hits counter driver circuitry. If a dropout occurs for less than the 10-millisecond interval, C6 is immediately clamped to ground by Q1, thus terminating its charging cycle.

The output of timing circuit Q1 and IC1B is applied to driver transistor Q403 and inhibit transistors Q410, 413, 416, which inhibit all the one-shot multivibrators during dropout intervals. The external dropout logic output is obtained from the collector of Q403 through isolation resistor R438.

The dropout threshold detector, IC403B, and its associated threshold level set control, R434, are not operational in the amplitude detector board.

4.2.16 PHASE/AMPLITUDE COINCIDENCE DETECTOR CIRCUITRY

Coincidence between the phase and amplitude hit threshold detectors is determined by transistor Q402. This transistor responds only when both inputs are positive, and triggers the coincidence multivibrator through C429. The external coincidence logic output is provided through isolating resistor R450.

4.2.17 COUNTER DRIVER CIRCUITRY

The totalizer driver circuitry is identical for the phase hits, amplitude hits, coincident and dropout counters, and indicator lamps. A detailed explanation is given for the amplitude hits totalizer, and this is used with appropriate substitution of component designations for the other driver circuits.

The transition in the threshold detector outputs is amplified in driver transistor Q401 and applied to input differentiating capacitor C431. The positive going edge is removed by D418 and the negative going pulse is applied through R470 to the multivibrator consisting of Q414, 415. The multivibrator provides the 50-millisecond on-pulse followed by a 50-millisecond off-time required for the mechanical counter operation. The multivibrator output is amplified by Q417, which feeds the counter driver Q418. Transient suppression for the output driver is provided by R479 and D419.

The output drives either counter L204 or indicator lamp DS203, depending on the position of COUNT-FLASH switch S207.

Inhibiting transistor Q416 is included in all except the dropout detector driver, and inhibits the multivibrator operation when a positive signal is obtained from timing circuit Q1, IC1B. Inhibit transistor Q413 for the phase hits multivibrator is located on the HLI-45 board.

4.2.18 TIMER

Mechanical timer S202 controls the dc voltage to the counters and indicator lamps through T201. When the timer is operating, timer on-off lamp DS205 is lit.

4.2.19 METER CIRCUIT

Input/output levels, peak-to-peak and average phase jitter, and frequency are monitored using front panel mounted, 50-microamp meter M201. The meter input is selected by meter switch S204. For input/output level monitoring, a bridge rectifier consisting of D201, 202 and R203, 204, 205 is used to rectify the audio voltages.

4.2.20 TRANSMIT OSCILLATOR

The transmit oscillator Q111 frequency is determined by LC tank circuit L102, C131. Its operation is similar to that of phase-locked reference oscillator Q104 (paragraph 4.2.7). Its output is connected to OUTPUT LEVEL control R215, which is connected to the push/pull emitter coupled amplifier, Q105, 106. This amplifier provides a low distortion, -20 to +10 dBm, 600-ohm test tone source for use in back-to-back and loop testing.

4.2.21 POWER SUPPLY

The power supply contains separate +15 and -15 volt dc regulator sections. It provides 0.01 percent line and 0.05 percent load regulation, and has a temperature coefficient of 0.02 percent per degree C. Noise and ripple on the power supply output measure 1.0 millivolt rms maximum.

The negative rectified voltage from D303, 304, and C302 is regulated by series power transistor Q301. The regulated voltage is compared to zener diode reference D306; and the difference is amplified by Q305, 308, 304 to provide the driving signal to Q301.

The positive voltage from D301, 302 and C301 is regulated by Q302. The reference is obtained from the negative supply; and differences are amplified by Q303, 305, 306 to provide the driving signal to Q302.

SECTION V

MAINTENANCE

5.1 MAINTENANCE PHILOSOPHY

Maintenance procedures for the Model 45 Phase Jitter Meter are divided into preventive and corrective classifications. Preventive maintenance consists of routine performance checks using the front panel controls of the instrument. Corrective maintenance covers symptom analysis, troubleshooting, repair, and calibration of the instrument.

5.2 PREVENTIVE MAINTENANCE

5.2.1 GENERAL

The preventive maintenance procedures described in the following paragraphs are used by the operator and maintenance personnel to verify proper instrument operation using the front panel controls and external test equipment. If proper operation is not achieved, refer to paragraph 5.3 for corrective maintenance procedures.

Periodic cleaning, lubrication, or inspection is not required.

The following routine tests are made with the INPUT selector switch set for voice frequency tests using the internal test oscillator as a signal input, or with the selector switch set for group frequency tests using an external signal generator whose exact frequency and level must be measured prior to the frequency translator test. Connections between the OUTPUT and INPUT terminals (red) are made using clip leads or an appropriate test cord.

5.2.2 INPUT/OUTPUT LEVEL CHECK

Set the meter switch to the OUTPUT LEVEL position and verify that the output level can be adjusted over a -20 to + 2 dBm range. Set the level to 0 dBm on the OUTPUT LEVEL position and then monitor the input level. The input level should be within ±0.5 dB of the output level indication.

Absolute calibration of the internal level meter is checked by comparison with an external standard meter connected in parallel across the INPUT terminals.

Set the meter switch to the LEVEL SET position and verify that the LEVEL SET control can be adjusted to provide a 0 dBm indication on the meter.

5.2.3 INPUT LEVEL CHECK (GROUP FREQUENCY)

Set the INPUT selector switch to the desired group frequency input position. Connect a test signal from the test signal generator to the GROUP FREQUENCY INPUT terminals and monitor its level with an appropriate external reference meter. Set the meter switch to the INPUT LEVEL position and verify that the meter indication is within ±0.5 dB of the external

reference meter. Be sure to make any necessary corrections in comparing the dBm indication (1 milliwatt across the characteristic input impedance of 150 ohms) to the voltage or dB calibrations on the external reference meter.

5.2.4 INPUT FREQUENCY CHECK (GROUP FREQUENCY)

Set the meter switch to the FREQ SET position and verify that the FREQ control can be adjusted to provide a proper frequency lock.

5.2.5 JITTER MEASUREMENT CHECK

Set the meter switch to the FREQ SET position and adjust the FREQ control as described in section III. Verify that both the P-P JITTER and AV JITTER positions of the meter switch indicate less than 1.5 degrees. A detailed calibration procedure of peak-to-peak and average phase jitter is contained in paragraph 5.3.4.

5.2.6 PHASE HITS CHECK

Rotate the timer control to the HOLD position and set the phase hits PEAK DEGREES switch to the 5 DEGREE position. Vary the FREQ control rapidly and observe that totalizer accumulates phase impulse counts.

5.2.7 AMPLITUDE HITS CHECK

Set the meter switch to the INPUT LEVEL position and adjust the OUTPUT LEVEL control for a 0-dBm indication with the INPUT switch set to the BRIDGE position and the INPUT selector switch to VF voice frequency. Set the meter switch to the LEVEL SET position and adjust the LEVEL SET control for a 0-dBm indication. Changing the setting of the INPUT switch between the BRIDGE and 600 OHM positions results in approximately a 6-dB input level change. Rotate the timer to the HOLD position and verify that amplitude hits are totalized in the 1-, 2-, and 3-dB positions of the ± DB switch as the INPUT switch is set back and forth between the 600 OHM and BRIDGE positions.

5.2.8 PHASE/AMPLITUDE COINCIDENT HITS CHECK

With the instrument adjusted as described in paragraphs 5.2.2 and 5.2.5, set the PEAK DEGREES switch to the 5^{O} position and the ± DB switch to the ±2 DB position. Verify that when the INPUT switch is set back and forth between BRIDGE and 600 OHM, and the FREQ control is simultaneously varied, both phase, amplitude, and coincident hits are detected and indicated. Setting the PEAK DEGREES switch to a level where phase hits are no longer detected, or alternately setting the ± DB switch at a threshold level of 6 dB causes the coincident indications to stop.

5.2.9 DROPOUTS CHECK

With the instrument adjusted in accordance with paragraph 5.2.2, remove the input signal (both input leads must be removed simultaneously). A dropout indication occurs 10 milliseconds after removal of the input signal.

5.3 CORRECTIVE MAINTENANCE

5.3.1 TROUBLESHOOTING

This section covers the symptom analysis, circuit level isolation, and calibration procedures of the Model 45 Phase Jitter Meter.

No specialized mechanical assembly or disassembly procedures are required. Accepted practices must be followed when repair is undertaken on main frame components or the printed circuit boards.

Recommended troubleshooting techniques are based on signal tracing methods where a known input signal is supplied and the level and waveform are verified as the signal progresses through the circuitry. Typical test equipment required to perform the troubleshooting procedures is listed in table 5-1.

Table 5-1. Test Equipment Required

ITEM	MODEL	QTY.
Audio oscillator	HP 204C	2
Resistor network	(See figure 5-1.)	1
AC voltmeter	HP 400EL	1
Oscilloscope, single channel, 1- MHz frequency response	Tektronix 323	1
Frequency counter, high impedance, low capacity probe	HP-5243 or HP-5245	1
Multimeter	Simpson 260	1

5.3.2 SYMPTOM ANALYSIS

The preventive maintenance checks of paragraph 5.2 are used to isolate the area in which a malfunction occurs. Table 5-2 summarizes possible fault locations for each of the preventive maintenance tests.

5.3.3 CIRCUIT LEVEL TROUBLESHOOTING

The following sections describe the general procedures to be used in locating malfunctions. Where appropriate, performance standards, i.e., voltage levels or waveform descriptions, are provided to assist in the troubleshooting procedures.

When a circuit has the proper input signal, but the correct output cannot be measured, the components associated with that circuit must be checked and replaced if defective. Failure in an integrated circuit can often be detected by feeling the case temperature.

WARNING

Normally, integrated circuits are moderately warm to the touch; however, when defective, they can become extremely warm, causing a painful sensation when touched.

Table 5-2. Symptom Analysis

PREVENTIVE MAINTENANCE TEST	PROBABLE TROUBLE LOCATIONS
1. No response from any test	a. AC power cord b. Internal ac wiring or POWER switch S203 c. Power supply
2. Input/output level check	a. Q105, 106, 111, R215 b. Meter switch S204 or meter rectifiers D201, 202 c. Meter M201
3. Input level check (group frequency)	a. INPUT selector switch S601 b. Q601, R613 c. IC601, 602
4. Input frequency check (group frequency)	a. (Refer to 5)
5. Jitter measurement check:	
Unable to "lock" frequency	a. Q103, 111 oscillator frequency incorrect b. IC-101AB, 102B, 401A, Q101, 102, 103, 104
No average jitter indication	a. IC-102A, 103A, 104B
No peak-to-peak jitter indication	a. IC-103B, D111, 112
6. Phase hits check	a. Totalizer power supply S202; T201; D115 thru D118 b. IC-104A; 501A; Q107, 108, 109, 110, 502 c. PEAK DEGREES switch S205 d. Totalizer L203

Table 5-2. Symptom Analysis (Cont)

PREVENTIVE MAINTENANCE TEST	PROBABLE TROUBLE LOCATIONS
7. Amplitude hits check:	
Cannot set LEVEL SET	a. IC401A, R223
Improper threshold detection	a. IC401B, 402, 403A, 404
No indication	a. IC501B, Q414 thru Q418, 501 b. L203, DS204, S202
8. Phase/amplitude coincidence check	a. Phase hits circuitry (Refer to 6) b. Amplitude hits circuitry (Refer to 7) c. Q402, 408 thru 412 d. L205, DS202, S202
9. Dropout check	a. IC1A, IC2A b. IC3A, IC3B c. IC2B d. Q1, IC1B e. Q403 thru 407 f. L206, DS201, S202

5.3.3.1 TEST TONE OUTPUT CIRCUITRY

The output test tone oscillator is best checked using an oscilloscope. Under normal operation, a 12-volt, peak-to-peak sine wave is present at terminals 44-R and 44-S, with the OUTPUT LEVEL control R215 in the full clockwise position. If outputs are not present, check Q111. Check tank inductor L102 for continuity and check tuning capacitor C131 for shorts.

If output is not present across terminals 44-P and 44-Q, check Q105, 106 and T101.

5.3.3.2 INPUT CIRCUITRY

The input circuitry is most easily checked using a 0-dBm, 1.0-kHz input test signal. With this test signal, verify that LEVEL SET control R223 can be adjusted to provide 0 dBm at the output (pin 2) of IC401A. If 0 dBm cannot be obtained, check diodes D401 through D404 for shorts. If the diodes are good, replace IC401A.

With this test signal, verify that a ±15 volt square wave of the same frequency is present at the output (pin 2) of IC-101A. If a square wave is not present at this output, check IC101A.

The input level meter is checked using the same input signal. The INPUT LEVEL and OUTPUT LEVEL meter positions indicate within ±0.5 dB of the standard level as measured by an external reference voltmeter. Check R203 through 205 and D201, 202 if this accuracy is not obtained.

5.3.3.3 FREQUENCY TRANSLATOR CIRCUITRY

Before detailed troubleshooting is undertaken, check for +15 volts at terminal P of the frequency translator board. The presence of the input signal can be verified using an oscilloscope at GROUP FREQUENCY INPUT connector TB601 and at terminals J and L of the frequency translator board. The input signal can also be verified between pin 12 of IC601 and ground. This signal is attenuated by input attenuater R601, R602, R603 and has a dc offset resulting from the bias voltage of pin 2.

Crystal oscillator performance is checked using an oscilloscope at pin 9 of IC601. When operating properly, a square wave of 0.15 volt peak-to-peak at the crystal oscillator frequency is observed at this point.

Using an oscilloscope, verify that an output signal is present at pin 14 of IC601. With no input signal applied, a 0.6-volt, peak-to-peak carrier signal is present; and, when a maximum level group frequency input signal is applied, the beat between the carrier signal and input frequency appears as an envelope on the combined signal at pin 14 of IC601.

The filtered IF signal can be observed with an oscilloscope at pin 3 of IF filter F601 (connected to R607), and is approximately 0.1 volt peak-to-peak with a high level group frequency input singal. Filter response is verified by varying the frequency of the input test signal and noting the attenuation of the filter response which takes place approximately 2.0 kHz either side of the center frequency. The signal at pin 3 does not entirely disappear due to the second translation oscillator feedthrough present at this point.

Oscillator performance of second frequency translator IC602 is monitored by observing the waveform at pin 9. This waveform is identical to that of the previous section. The second frequency translator output is observed at pin 1 of IC602, and consists of the translation oscillator signal and the 1.0-kHz output signal. With maximum test signal input, approximately a 4-volt, peak-to-peak signal is present at the junction of R609, C619. This signal has a voltage offset of approximately 8.0 volts dc.

Depending upon the setting of output gain control R613, the audio output amplifier, Q601, has a gain of less than 1. The 1-kHz signal output level can be observed at terminal B of the frequency translator board.

5.3.3.4 PHASE-LOCK OSCILLATOR

The phase-lock oscillator circuit incorporates phase detector Q101, 102; high pass filter IC-102B; reactance modulator Q104; LC oscillator Q103; and reference limiter IC-101B.

With no input signal, check for a 10-volt, or greater, peak-to-peak sine wave at pin 8, of IC-101B and a ±15 volt square wave at pin 12 of IC-101B. Verify that the frequency is 1-kHz ±5 Hz (adjust FREQ control for proper frequency). If waveforms are not present, check Q103 and IC-101B.

Connect a 1.0-kHz test signal to the INPUT; and using an oscilloscope, verify that a ±6 volt pulse train is present at the junction of R111-112 with the instrument in the frequency "locked" condition. The pulse widths are a function of the input and reference signal phase relationship. Place the instrument in an "out-of-lock" condition; and, using an oscilloscope, monitor the output level of IC-102B (pin 12). The output varies over a range of approximately ±6 volts, and appears as an isosceles waveform at the "beat" frequency. If the output of

IC-102B remains constant in the "out-of-lock" condition, replace IC-102. If this output is proper, and frequency "lock" cannot be obtained, check Q104.

5.3.3.5 PEAK-TO-PEAK AND AVERAGE PHASE DETECTOR

The output of IC-102B is coupled and then amplified and filtered in IC-102A with a gain of 2. The gain is verified using an oscilloscope.

Operation of full wave rectifier IC-103A, 104B is verified using the 11.5-degree, peak-to-peak jitter calibration signal (paragraph 5.3.4.4) and monitoring the waveform at the output of IC-104B. The waveform is a full wave rectified replica of the output of IC-102A. If no output or a fixed level of ±15 volts is measured, replace IC-103 and IC-104.

The output of IC-103A is used to drive the peak-to-peak detector and its unity gain buffer amplifier IC-103B. Using an oscilloscope, verify that the output of IC-103B (pin 12) matches its input from IC-103A (pin 2). Under the test conditions of a 11.5-degree, peak-to-peak jitter input, dc voltages of approximately 3 volts are measured on the load side of D111 or D112.

5.3.3.6 PHASE IMPULSE DETECTOR

A Schmidt trigger configuration of IC-104A is used to detect phase variations which exceed the threshold set by PEAK DEGREES switch S205. When operating properly, the output of IC-104A (pin 2) changes from +15 volts to -15 volts whenever the input signal at R147 (IC-104A, pin 5) exceeds the dc level established by the resistor divider chain of S205. Oscilloscope observations of dc levels and waveforms are utilized to verify operation of the detector circuit using the 11.5-degree, peak-to-peak jitter calibration signal of paragraph 5.3.4.4, with S205 set in the 5-degree threshold position. The detector output is connected to the time out board, where Q502 clamps C502 to ground when +15 V dc is applied to terminal D. Using an oscilloscope, verify that C502 charges towards +15 V dc during the hit period. If this does not occur, replace Q502. By increasing the level of oscillator No. 2, the hit period is extended beyond 4.0 milliseconds; at which point a +15 volt to -15 volt transition takes place at the output of IC501A (terminal C) for the remainder of each hit period. If this does not occur, replace IC501. This output is differentiated by C122 and the negative-going edge used to trigger the one-shot multivibrator which drives phase mechanical totalizer L203. Verify with an oscilloscope that the negative trigger spike across D113 exceeds 10 volts.

5.3.3.7 AUTOMATIC LEVEL CONTROL (ALC)

The automatic level control (ALC) consists of voltage controlled attenuator Q421, R406; full wave rectifier IC-401B, IC-402A; and peak detector D409, C411. With a 1.0-kHz test-tone input, adjust LEVEL SET control R223 for a 0-dBm meter indication in the LEVEL SET position. Using a dc voltmeter, check the voltage at the junction of diode D409 and C411. This voltage is between +2 and +3.5 volts dc. If this voltage is not obtained, replace Q421 and adjust R418 in accordance with the calibration procedures of paragraph 5.3.4. If the correct dc voltage is still not obtained, replace IC401B and IC402A.

Verify with an oscilloscope that a full-wave rectified sine wave appears at the output (pin 2) of IC402A. The peak value of the full-wave is approximately 3 volts. Using a voltmeter, verify that approximately -1 volt dc is present at the output (pin 12) of IC402B. If a sine wave is not displayed, or if ±15 volts is measured, replace IC402

5.3.3.8 AMPLITUDE HITS DETECTOR

The amplitude hits detector consists of reference amplifier IC403A; positive hits detector IC404A; negative hits detector IC404B; and combining diodes D410, 411.

Using the 0-dBm test signal, measure the voltage appearing at pin 6 of IC403A. The output voltage (pin 2) of this amplifier is twice the voltage measured at pin 6. If voltage is not obtained, replace IC403A. If an incorrect voltage is obtained, check the resistor values R216 through 222. Under normal conditions, the voltage at pin 6 of IC403A is approximately 2 volts and the voltage at pin 2 approximately 4 volts.

Operation of the positive and negative hit threshold detectors is verified by observing their output (pin 2 and pin 12, respectively) on an oscilloscope with the ± dB switch set at ±2 dB. The INPUT BRIDGE-600 OHM switch is used to increase and decrease the signal level. An increase in signal level causes the output of IC404A to change from -15 volts to +15 volts. If this is not observed, replace IC404. A decrease in signal level of 2 dB or greater causes the output of negative detector IC-404B to change from -15 to +15 volts dc. If this does not occur, replace IC404. The detector outputs are combined by diodes D410, 411 and are connected to the time out board where Q501 clamps C501 to ground when no hits are detected. Verify with an oscilloscope that C501 charges toward -15 V dc during a hit period. If this does not occur, replace Q501. When the hit duration exceeds 4.0 milliseconds, the output of IC501B changes from -15 volts to +15 volts for the remainder of each hit duration. If this does not occur, replace IC501.

5.3.3.9 PHASE/AMPLITUDE COINCIDENT DETECTOR

The coincident detector consists of Q402, which functions as an AND gate supplying a negative going output only when both the phase and amplitude inputs are positive.

Set up the test conditions described in paragraph 5.2.8 and verify that -15 to +10 volt logic pulses are applied to the base of Q402, and 0 to +10 volt pulses are applied to the base of Q113. Verify that 0 to -10 volt pulses appear across D412. If pulses are not present, replace Q402, 113.

5.3.3.10 DROPOUT DETECTOR

The dropout detector consists of full wave amplitude detector IC1A and IC2A; 300-Hz, low-pass filter IC3A and IC3B; threshold detector IC2B; and timing circuit Q1 and IC1B.

Apply a 0-dBm test signal to the INPUT terminals of the instrument. This signal is present at terminal D, input of IC1A. Using an oscilloscope, observe a full-wave rectified sine wave at pin 1 of IC2A. The test signal at this point represents the peak value of the input test signal at pin 2 of IC1A. If a sine wave of insufficient amplitude is displayed on the oscilloscope, or is not displayed, replace IC1A, IC2A or associated circuit components as necessary.

Using a voltmeter, measure 6-dB gain at output (pin 7) of low-pass filter IC3B. If this increase in the test signal is not obtained, replace IC3A, IC3B or associated circuit components as necessary.

Set the instruments LEVEL SET control for 0 dBm with the meter switch set to the LEVEL SET position. When adjusted for a dropout threshold of -12 dB (paragraph 5.3.4.7), the voltage at C6 is -15 V dc. Disconnect, simultaneously, both input signal leads from the INPUT terminals and then measure the voltage at C6. If the voltage is not -15 V dc, replace Q1.

When the output of IC1B changes from - to + 15 volts, the voltage at the junction of Q403 and R437 changes from 0 to -10 volts. If -10 volts is not indicated, replace Q403.

If dropout does not occur after 10 milliseconds from the time that the input test signal leads are disconnected, replace C6 and/or R21 as necessary.

5.3.3.11 TIMER

Operation of the mechanical counters or indicating lights is controlled by mechanical timer S202. To verify its operation, connect a dc voltmeter between ground and pin 45-K. Verify that approximately 28 volts dc is present when the timer is in the ON or HOLD position. If voltage is not present, check timer S202, transformer T202, and diodes D119 through 122.

5.3.3.12 COUNTER DRIVERS

Multivibrator circuit values are arranged to provide an "on" time of 50 milliseconds. The following procedure is used for any of the counter drivers. A negative spike, multivibrator trigger input of 15 volts is observed at the anode of D113. The output is observed at the base of Q109 with an oscilloscope for measurements of proper "on" and "off" pulse durations. This pulse is amplified in Q109 and drives Q110 which actuates the totalizer. A multitester is used to measure the dc supply voltage (between 25 and 30 volts dc) from bridge rectifier D115 through D118.

5.3.3.13 POWER SUPPLY

The power supply provides regulated +15 V dc and -15 V dc. These voltages are verified using a multimeter and must be within ±0.5 volt. Improper output voltages are caused by excessive current drain due to a failure elsewhere in the unit. This is determined by temporarily disconnecting the supply leads from pins 1 and 10 and again measuring the supply voltages. Normal loading is simulated using a 170-ohm, 2-watt resistor connected to ground.

If proper voltages are not obtained from the power supply, check diodes D311, 312 for shorts. Verify that +28 V dc is present at the junction of D301, 302 and R311, and -28 V dc at D303, 304, and R301. If this is not obtained, check transformer T301; diodes D301 through 304; and capacitors C301, 302.

If the previous checks are satisfactory, each transistor, diode, and resistor must be individually checked. Components associated with the -15 V dc regulator section are measured first, followed by those of the +15 V dc regulator.

5.3.4 CALIBRATION

The following procedures are used to calibrate the test tone output frequency, input/output level monitor meter, reference oscillator frequency, peak-to-peak and average phase jitter circuits, phase impulse counter, amplitude hits detector, dropout detector threshold, and the frequency translator oscillators and overall gain. Calibration is normally required when maintenance has been performed on the associated circuitry which affects the instrument's operation or when there is reason to suspect the calibration is no longer accurate.

5.3.4.1 TEST TONE OUTPUT FREQUENCY

a. Connect frequency counter (capable of measuring 1000 kHz) to the OUTPUT terminals.

b. Adjust the OUTPUT LEVEL control until the counter is stabilized.

c. Adjust L102 (printed circuit board mounted inductor) to obtain an output frequency of 1.0 kHz ±1 Hz.

5.3.4.2 INPUT/OUTPUT LEVEL METER

a. Connect the test tone OUTPUT terminals to the INPUT terminals.

b. Adjust OUTPUT LEVEL control for a 0-dBm indication in the 600 OHM position.

c. Connect a standard reference meter in parallel with the INPUT terminals. Be sure all ground connections are properly made.

d. Select the value of R203 (located on S204) to provide an indication within 0.25 dB of the reference meter.

5.3.4.3 REFERENCE PHASE LOCKED OSCILLATOR FREQUENCY

a. Connect a 0-dBm input signal at a frequency of 1.0 kHz to the INPUT terminals.

b. Adjust the LEVEL SET control in accordance with paragraph 3.3.3.

c. Rotate the FREQ control to its midrange position (indicator dot straight up).

d. Adjust L101 (printed circuit board mounted inductor) to obtain a meter indication at the FREQ SET mark with the meter switch in the FREQ SET position. L101 is adjusted using a small screwdriver to turn the adjustor slug reached through the hole in the center of the core assembly.

5.3.4.4 PEAK-TO-PEAK AND AVERAGE PHASE JITTER

a. The peak-to-peak and average phase jitter ranges are calibrated using a two-tone audio technique where the phase jitter is proportional to the level difference between the two tones.

b. To perform this calibration, two audio oscillators having 1 percent or less harmonic distortion are connected to a resistive network as shown in figure 5-1. Precision resistors of 1 percent tolerance are required for this network.

c. Adjust oscillator No. 2 level to minimum and adjust the No. 1 oscillator to provide 0 dBm at a frequency of 1 kHz (±5 Hz) at the input of the Model 45 Phase Jitter Meter. Measure the level of oscillator No. 1 across its output terminal using a level meter or a selective voltmeter.

d. Adjust the frequency of oscillator No. 2 to 1030 Hz (±5 Hz).

e. Using the voltmeter, adjust the oscillator No. 2 level at its output so that it is 20 dB below the output of oscillator No. 1 as measured at its output terminals (as listed in table 5-3).

Table 5-3. Phase Jitter Calibration Chart

LEVEL DIFFERENCE	JITTER		
Between Oscillators 1 and 2	Peak-to-Peak	Peak	Average
20.0 dB[1]	11.5°	5.7°	3.6°
11.7 dB[2]	30.0°	15.0°	9.6°

1. Used for peak-to-peak jitter calibration (R146).

2. Used for average jitter and phase impulse counter calibration (R139 and R148).

f. Adjust the FREQ control of the Model 45 Phase Jitter Meter for the "locked" condition and note the value of peak-to-peak phase jitter. If this differs by more than 1.0 degree from 11.5 degrees, adjust R145 to provide the proper meter indication.

g. Adjust audio oscillator No. 2 for a level of 11.7 dB below oscillator No. 1. The average jitter indication should be within 1.0 degree of 9.2 degrees. If this indication is not obtained, adjust R139 to provide the proper meter indication.

Note

The Model 45 Phase Jitter Meter's test tone oscillator can be used as oscillator No. 1. However, the use of two external oscillators is recommended.

5.3.4.5 PHASE IMPULSE DETECTOR

a. Calibration of the phase impulse detector is made in a manner similar to that of the phase jitter calibration. The calibration arrangement as shown in figure 5-1 is used.

b. Perform steps a through d and f of paragraph 5.3.4.4.

c. Set the PEAK DEGREES switch to the 15° position, and rotate the TIMER control to the HOLD position.

d. Adjust oscillator No. 2 for a level 11.7 dB below oscillator No. 1.

e. Connect an oscilloscope to terminal M of the HLI-44 board.

f. Adjust R148 so that pulses from +15 volts to -15 volts just begin to appear.

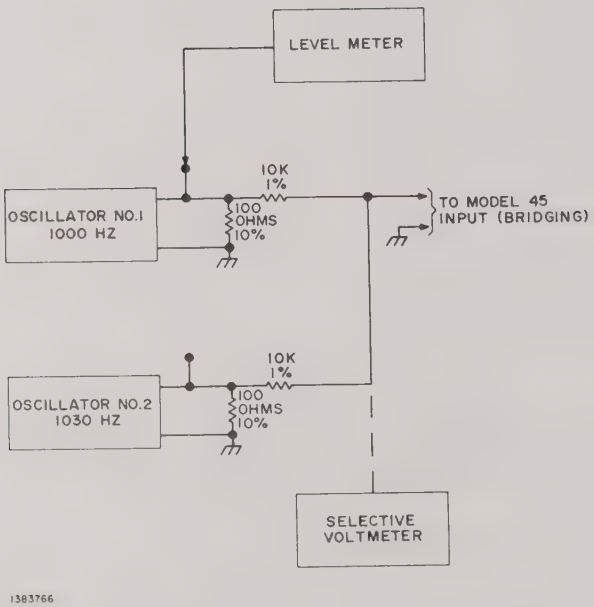


Figure 5-1. Calibration, Block Diagram

5.3.4.6 AMPLITUDE HITS

The calibration of the threshold levels of the amplitude hits detector is fixed by the resistor values R219 through 222, 425, 426; and therefore no calibration adjustments are provided. It is necessary, however, to adjust the automatic level control circuitry for optimum operation in accordance with the following procedures.

a. Using a 1.0-kHz, test-tone input, properly adjust the LEVEL SET control.

b. Connect a dc voltmeter to the junction of D409 and C411 on the HLI-45 board.

c. Adjust potentiometer R418 for a positive voltage indication of 2.5 volts dc. Wait approximately 10 to 15 seconds before reading the voltmeter to allow the long-time constant circuitry to come to its final value.

5.3.4.7 DROPOUT THRESHOLD

a. Adjust the instrument in accordance with paragraph 5.2.2.

b. Without adjusting the LEVEL SET control, lower the input level 12 dB. The internal level meter can be used, but more accurate indications are obtained using an external reference voltmeter connected across the INPUT terminals.

c. Using an oscilloscope or voltmeter, monitor the voltage at the dropout logic output (TB 203).

d. Adjust potentiometer R17 to cause a change in the output level (either 0 or -10 volts). Adjust R17 to the position which causes the level to change from 0 to -10 volts.

5.3.4.8 TRANSLATION OSCILLATOR FREQUENCY

a. When adjusting the translation oscillator frequency, the fixed second translation oscillator is always adjusted first. The input oscillators are then adjusted to provide the desired overall response. Set the INPUT selector switch to the group frequency position.

b. Using a frequency counter with a high input impedance and a low capacity probe, monitor the second fixed oscillator frequency at pin 9 of IC602. Adjust trimmer capacitor C606 to provide an oscillator frequency of 454 kHz.

Note

Further adjustment of the second translation oscillator for the remainder of the calibration procedure is not required.

c. Set the INPUT selector switch to the VF (voice frequency) position; set the INPUT switch to the 600 OHM position. Using a voice frequency input signal of 1010 Hz ±1 Hz, adjust the FREQ control to provide the proper meter indication in the VF (voice frequency) input mode.

d. Connect an input signal to the GROUP FREQUENCY INPUT terminals; and, using a frequency counter for monitoring, adjust the input signal within ±1 Hz of the desired frequency.

Note

Do not change the setting of the FREQ control when performing step e.

e. Set the INPUT selector switch to the desired group frequency position and adjust the appropriate trimmer of first translation oscillator IC601 to provide the proper frequency indication on the meter.

f. Change the test signal frequency, and adjust the remaining group frequency input positions in a similar manner (steps d and e).

5.3.4.9 TRANSLATOR GAIN

a. Connect a proper frequency input singal to the GROUP FREQUENCY INPUT terminals and set its level to 0 dBm, referenced to the group input impedance (150 ohms).

b. Set the METER switch to the INPUT LEVEL position and adjust R613 for a meter indication of 0 dBm.

5.4 PARTS LISTS

The parts lists contain information for ordering replacement parts for the Model 45 Phase Jitter Meter. The parts lists for the main frame assembly and its subassemblies are listed in tables 5-4 through 5-10. The location of the parts on the main frame is referenced to the Model 45 wiring diagram, figure 5-2. The location of all the other parts are shown in figures 5-4, 5-6, 5-8, 5-10, and 5-12.

5.5 DRAWINGS

Figure 5-2 is the wiring diagram of the Model 45 Phase Jitter Meter. Figures 5-3, 5-5, 5-7, 5-9, and 5-11 are the schematic diagrams of its subassemblies.

Table 5-4. Parts List, Main Frame

FIG. NO.	REF. DESIG.	DESCRIPTION	PART NO.	MFR.
5-2	D201, 202	DIODE, germanium, 1N191	--	GE
	DS201 thru DS205	LAMP, pilot, incandesent 28 V, 0.040 A	327	Chicago Lamp
	DS206	LAMP, pilot, neon NE-2D	--	Chicago Lamp
	L203 thru L206	TOTALIZER, 24 V dc, 4 digit	TCeZ4E	Sodeco
	M201	METER, 0-50 microamp	44-001	HLI
	R201	RESISTOR, fixed, composition, 620 ohm, ±5%, 2 W	--	Ohmite
	R202	RESISTOR, variable, carbon, 10K, ±10%, 1/2 W	ASM	Ohmite
	R203	RESISTOR, fixed, composition, selected valve, ±5%, 1/4 W	--	Ohmite
	R204, 205	RESISTOR, fixed, composition, 10K, ±5%, 1/4 W	--	Ohmite
	R206 thru R214	RESISTOR, fixed, composition, 150 ohm, ±1%, 1/4 W	RN60D	IRC
	R215	RESISTOR, variable, carbon, 10K, ±10%, 1/2 W	ASM	Ohmite
	R216	RESISTOR, fixed, deposited, 576 ohm, ±1%, 1/4 W	RN60D	IRC
	R217	RESISTOR, fixed, deposited, 154 ohm, ±1%, 1/4 W	RN60D	IRC
	R218	RESISTOR, fixed, deposited, 137 ohm, ±1%, 1/4 W	RN60D	IRC
	R219	RESISTOR, fixed, deposited, 97.6 ohm, ±1%, 1/4 W	RN60D	IRC
	R220	RESISTOR, fixed, deposited, 86.6 ohm, ±1%, 1/4 W	RN60D	IRC
	R221	RESISTOR, fixed, deposited, 205 ohm, ±1%, 1/4 W	RN60D	IRC
	R222	RESISTOR, fixed, deposited, 499 ohm, ±1%, 1/4 W	RN60D	IRC
	R223	RESISTOR, variable, carbon, 100K/100K, ±10%, 2 W	CCU	Ohmite
	R224	RESISTOR, fixed, composition, 610 ohm, ±5%, 2 W	--	Ohmite

Table 5-4. Parts List, Main Frame (Cont)

FIG. NO.	REF. DESIG.	DESCRIPTION	PART NO.	MFR.
5-2	R225	RESISTOR, fixed, composition, 27K, ±5%, 1/4 W	--	Ohmite
	S201	SWITCH, toggle, 1 pole, 2 position	MST 115D	Alco
	S202	SWITCH, timer, 60-minute with hold, 1 pole, 1 position	90024	M.H. Rhodes
	S203	SWITCH, push, 1 pole, 2 position	616	Marco-Oak
	S204	SWITCH, rotary, 4 pole, 6 position	PA1015	Centralab
	S205	SWITCH, rotary, 1 pole, 9 position	PA1000	Centralab
	S206	SWITCH, rotary, 2 pole, 4 position	PA1002	Centralab
	S601	SWITCH, rotary, 4 pole, 6 position	PSA-211	Centralab
	T201	TRANSFORMER, power	P8395	Stancor

Table 5-5. Parts List, Phase Jitter Detector Board

FIG. NO.	REF DESIG.	DESCRIPTION	PART NO.	MFR.
5-4		PHASE JITTER DETECTOR BOARD	HLI 44-3	
	C101, 102	CAPACITOR, paper 0.22 μF, 200 V dc (not used in Model 45)	2PS-P22	Sprague
	C103	CAPACITOR, ceramic, 0.01 μF, 50 V dc	HY	Sprague
	C104	CAPACITOR, electrolytic, 50 μF, 25 V dc	30D	Sprague
	C105	CAPACTIOR, paper, 0.15 μF, 75 V dc	225PZ	Sprague
	C106	CAPACITOR, paper, 0.018 μF, 100 V dc	225PW	Sprague
	C107	CAPACITOR, ceramic 47 pF, 1000 V dc	5GA	Sprague
	C108	Same as C107		
	C109	CAPACITOR, tantalum, 22 μF, 15 V dc	TAS	Mallory
	C110	CAPACITOR, paper, 0.22 μF, 75 V dc	225PZ	Sprague
	C111	Same as C109		
	C112	Same as C107		
	C113, 114	Same as C103		
	C115	Same as C107		
	C116	Same as C103		
	C117	Same as C107		
	C118	Same as C103		
	C119	Same as C107		
	C120, 121	Same as C104		
	C122	CAPACITOR, ceramic, .001 μF, 600 V dc	5GA	Sprague
	C123	Same as C110		
	C124	CAPACITOR, ceramic, 2.2 μF, 20 V dc	5CO	Sprague
	C125	CAPACITOR, paper, 0.039 μF, 100 V dc	225W	Sprague
	C126	CAPACITOR, paper, 0.027 μF, 100 V dc	225W	Sprague
	C127	CAPACITOR, paper, 0.01 μF, 100 V dc	225W	Sprague

Table 5-5. Parts List, Phase Jitter Detector Board (Cont)

FIG. NO.	REF. DESIG.	DESCRIPTION	PART NO.	MFR.
5-4	C128	CAPACITOR, paper, selected valve, 100 V dc	225W	Sprague
	C129	Same as C105		
	C130	Same as C107		
	C131	Same as C110		
	C132, 133	Same as C110		
	C135	CAPACITOR, paper, 0.2 μF, 200 V dc	220P	Sprague
	C136, 137	Same as C103		
	C138, 139	CAPACITOR, electrolytic, 150 μF, 16 V dc (not used in Model 45)	30D	Sprague
	C140	Same as C106		
	D101 thru D104	DIODE, silicon, 1N3064 (not used in Model 45)	--	Fairchild
	D105, 106	DIODE, silicon, 1N3064	--	Fairchild
	D107, 108	DIODE, zener, 1N706A	--	Motorola
	D109 thru D114	Same as D105		
	D115 thru D118	DIODE, silicon, 1N2482	--	Sarkes-Tarzian
	D119 thru D121	Same as D105		
	IC 101 thru IC 104	INTEGRATED CIRCUIT, dual amplifier	MC-1437L or TOA 2809	Motorola Transistron
	L101, 102	INDUCTOR, pot core (adj.), 0.1 mH	44-008	HLI
	Q101 thru Q107	TRANSISTOR, silicon, 2N3566	--	Fairchild
	Q108	TRANSISTOR, silicon, 2N5138	--	Fairchild
	Q109	Same as Q101		
	Q110	TRANSISTOR, silicon, 2N3440	--	RCA
	Q111	Same as Q101		
	R101	Same as R103		
	R103	RESISTOR. fixed, composition, 10K, ±5%, 1/4 W	--	Ohmite

Table 5-5. Parts List, Phase Jitter Detector Board (Cont)

FIG. NO.	REF. DESIG.	DESCRIPTION	PART NO.	MFR.
5-4	R104	RESISTOR. fixed, composition, 100K, ±5%, 1/4 W	--	Ohmite
	R105	Same as R103		
	R106	RESISTOR. fixed, composition, 2.2K, ±5%, 1/4 W	--	Ohmite
	R107	RESISTOR. fixed, composition, 47K, ±5%, 1/4 W	--	Ohmite
	R108	RESISTOR. fixed, composition, 4.7K, ±5%, 1/4 W	--	Ohmite
	R109	Same as R107		
	R110	Same as R108		
	R111	Same as R103		
	R112	RESISTOR. fixed, composition, 1.0K, ±5%, 1/4 W	--	Ohmite
	R113	RESISTOR. fixed, composition, 13K, ±5%, 1/4W	--	Ohmite
	R114	RESISTOR. fixed, composition, 6.8K, ±5%, 1/4 W	--	Ohmite
	R115	RESISTOR. fixed, composition, 13K, ±5%, 1/4 W	--	Ohmite
	R116	Same as R106		
	R117	RESISTOR. fixed, composition, 2.7K, ±5%, 1/4 W	--	Ohmite
	R118	RESISTOR. fixed, composition, 220K, ±5%, 1/4 W	--	Ohmite
	R119	RESISTOR. fixed, composition, selected value, ±5%, 1/4 W	--	Ohmite
	R120	Same as R103		
	R121	RESISTOR. fixed, composition, 27K, ±5%, 1/4 W	--	Ohmite
	R123	Same as R106		
	R124	RESISTOR. fixed, composition, 12K, ±5%, 1/4 W	--	Ohmite
	R125	RESISTOR. fixed, composition, 27K, ±5%, 1/4 W	--	Ohmite
	R126	RESISTOR. fixed, composition, 22K, ±5%, 1/4 W	--	Ohmite

Table 5-5. Parts List, Phase Jitter Detector Board (Cont)

FIG. NO.	REF DESIG.	DESCRIPTION	PART NO.	MFR.
5-4	R127	RESISTOR. fixed, deposited, 10K, ±1%, 1/4 W	RN60D	IRC
	R128	Same as R108		
	R129	Same as R127		
	R130	Same as R127		
	R131	RESISTOR. fixed, deposited, 20K, ±1%, 1/4 W	RN60D	IRC
	R132	Same as R127		
	R133	Same as R106		
	R134	Same as R103		
	R135	RESISTOR. fixed, composition, 6.8K, ±5%, 1/4 W	--	Ohmite
	R136	Same as R131		
	R137	Same as R106		
	R138	RESISTOR. fixed, composition, 68K, ±5%, 1/4 W	--	Ohmite
	R139	RESISTOR. variable, wirewound, 20K, ±10%, 1/2 W	89PR203	Helipot
	R140	Same as R103		
	R141	Same as R126		
	R142	Same as R106		
	R143, 144	Same as R104		
	R145	Same as R139		
	R146	Same as R138		
	R147	Same as R106		
	R149	Same as R112		
	R148	RESISTOR. variable, wirewound, 1.0K, ±10%, 1/2 W	89PR102	Helipot
	R150	RESISTOR. fixed, composition, 1.8K, ±5%, 1/4 W	--	Ohmite
	R151	Same as R126 (not used in Model 45)		
	R152	Same as R127 (not used in Model 45)		
	R153	RESISTOR. fixed, composition, 120K, ±5%, 1/4 W	--	Ohmite
	R155	Same as R126		

Table 5-5. Parts List, Phase Jitter Detector Board (Cont)

FIG. NO.	REF. DESIG.	DESCRIPTION	PART NO.	MFR.
5-4	R156	Same as R104		
	R157	Same as R135		
	R158, 159	Same as R126		
	R160	Same as R108		
	R161	Same as R104		
	R162	Same as R104		
	R163	Same as R107		
	R164, 165	Same as R103		
	R166, 167	Same as R104		
	R168	Same as R106		
	R170, 171	RESISTOR. fixed, composition, 560 ohm, ±5%, 1/4 W	--	Ohmite
	R172, 173	Same as R104		
	R174, 175, 176	Same as R106		
	R177	Same as R112		
	R178	Same as R108		
	R179, 180	RESISTOR. fixed, composition, 100 ohm, ±5%, 1/4 W	--	Ohmite
	R181	RESISTOR. fixed, composition, 2.2 megohm, ±5%, 1/4 W	--	Ohmite
	T101	TRANSFORMER, audio	DCM9-PC	Microtran

Table 5-6. Parts List, Amplitude Detector Board

FIG. NO.	REF DESIG.	DESCRIPTION	PART NO.	MFR.
5-6		AMPLITUDE DETECTOR BOARD	HLI 45-3	
	C401, 402	CAPACITOR, paper, 0.22 μF, 200 V dc	2PS-P22	Sprague
	C403	CAPACITOR, ceramic disc, 47 pF, 1000 V dc	5GA	Sprague
	C404	CAPACITOR, ceramic disc, 0.01 μF, 50 V dc	HY	Sprague
	C405	CAPACITOR, electrolytic, 5 μF, 25 V dc	30-D	Sprague
	C406	Same as C404		
	C407	Same as C403		
	C408	CAPACITOR, electrolytic, 50 μF, 25 V dc	30-D	Sprague
	C409	Same as C404		
	C410	Same as C403		
	C411, 412	CAPACITOR, paper, 0.22 μF, 75 V dc	225P	Sprague
	C413	CAPACITOR, paper, 0.15 μF, 75 V dc	225P	Sprague
	C414	CAPACITOR, paper, 0.018 μF, 100 V dc	225P	Sprague
	C415	Same as C403		
	C416	Same as C404		
	C417	Not used		
	C418	Same as C403		
	C419	Same as C404		
	C420	Same as C408		
	C421	Same as C403		
	C422	CAPACITOR, ceramic disc, 0.001 μF, 1000 V dc	5GA	Sprague
	C423	Same as C403		
	C424	Same as C422		
	C425	Same as C403		
	C426, 427	Same as C422		
	C428	Same as C411		

Table 5-6. Parts List, Amplitude Detector Board (Cont)

FIG. NO.	REF. DESIG.	DESCRIPTION	PART NO.	MFR.
5-6	C429	Same as C422		
	C430	Same as C411		
	C431	Same as C422		
	C432	Same as C411		
	C433, 434	Same as C411		
	D401 thru D419	DIODE, silicon, 1N3064	--	Fairchild
	IC-401 thru IC-404	INTEGRATED CIRCUIT, dual amplifier	MC1437L or TOA 2809	Motorola Transitron
	Q401 thru Q403	TRANSISTOR, silicon, 2N5138	--	Fairchild
	Q404	TRANSISTOR, silicon, 2N3566	--	Fairchild
	Q405	Same as Q401		
	Q406	Same as Q404		
	Q407	TRANSISTOR, silicon, 2N3440	--	RCA
	Q408	Same as Q404		
	Q409	Same as Q401		
	Q410, 411	Same as Q404		
	Q412	Same as Q407		
	Q413, 414	Same as Q404		
	Q415	Same as Q401		
	Q416, 417	Same as Q404		
	Q418	Same as Q407		
	Q419, 420	Not used		
	Q421	TRANSISTOR, silicon, MPF102	--	Motorola
	R401, 402	RESISTOR, fixed, composition, 10K, ±5%, 2 W	--	Ohmite
	R403, 404	RESISTOR, fixed, composition, 4.7K, ±5%, 1/4 W	--	Ohmite
	R405	RESISTOR, fixed, composition, 2.2K, ±5%, 1/4 W	--	Ohmite
	R406	RESISTOR, fixed, composition, 100K, ±5%, 1/4 W	--	Ohmite
	R407	Same as R405		

Table 5-6. Parts List, Amplitude Detector Board (Cont)

FIG. NO.	REF DESIG.	DESCRIPTION	PART NO.	MFR.
5-6	R408	RESISTOR, fixed, composition, 10K, ±5%, 1/4 W	--	Ohmite
	R409 thru R412	RESISTOR, fixed, deposited, 20K, ±1%, 1/4 W	RN60D	IRC
	R413	RESISTOR, fixed, composition, 51 ohm, +5%, 1/4 W	--	Ohmite
	R414	Same as R405		
	R415	RESISTOR, fixed, composition, 51K, ±5%, 1/4 W	--	Ohmite
	R416	RESISTOR, fixed, composition, 2.2 megohm, ±5%, 1/4 W	--	Ohmite
	R417	Same as R406		
	R418	RESISTOR, variable, wire wound, 20K, 10%, 1/2 W	89PR203	Helipot
	R419	RESISTOR, fixed, composition, 3.3K, ±5%, 1/4 W	--	Ohmite
	R420	RESISTOR, fixed, composition, 16K, ±5%, 1/4 W	--	Ohmite
	R421	RESISTOR, fixed, composition, 8.2K, ±5%, 1/4 W	--	Ohmite
	R422	Same as R420		
	R423	Same as R405		
	R424	Same as R408		
	R425	RESISTOR, fixed, deposited, 120 ohm, ±1%, 1/4 W	RN60D	IRC
	R426	RESISTOR, fixed, deposited, 110 ohm, ±1%, 1/4 W	RN60D	IRC
	R427	Same as R405		
	R428	RESISTOR, fixed, composition, 1.8K, ±5%, 1/4 W	--	Ohmite
	R429	Same as R416		
	R430	Same as R428		
	R431	Same as R416		
	R432	RESISTOR, fixed, composition, 6.8K, ±5%, 1/4 W	--	Ohmite
	R433	RESISTOR, fixed, composition, 300 ohm, ±5%, 1/4 W	--	Ohmite

Table 5-6. Parts List, Amplitude Detector Board (Cont)

FIG. NO.	REF. DESIG.	DESCRIPTION	PART NO.	MFR.
5-6	R434	RESISTOR, variable, wire wound, 200 ohm, ±10%, 1/2 W	89PR200	Helipot
	R435	Not used		
	R436, 437	Same as R403		
	R438	Same as R408		
	R439	RESISTOR, fixed, composition, 33K, ±5%, 1/4 W	--	Ohmite
	R440	RESISTOR, fixed, composition, 22K, ±5%, 1/4 W	--	Ohmite
	R441	Same as R406		
	R442	Same as R432		
	R443	Same as R403		
	R444, 445	Same as R440		
	R446	RESISTOR, fixed, composition, 1K, ±5%, 1/4 W	--	Ohmite
	R447	Same as R408		
	R448	Same as R440		
	R449	Same as R403		
	R450	Same as R408		
	R451	Same as R403		
	R452	Same as R408		
	R453	Same as R439		
	R454	Same as R440		
	R455	Same as R406		
	R456	Same as R432		
	R457	Same as R403		
	R458, 459	Same as R440		
	R461	Same as R403		
	R462	Same as R408		
	R463	Not used		
	R464	Same as R408		
	R465	Same as R446		
	R466	Same as R408		
	R467	Same as R440		

Table 5-6. Parts List, Amplitude Detector Board (Cont)

FIG. NO.	REF. DESIG.	DESCRIPTION	PART NO.	MFR.
5-6	R468	Same as R403		
	R469	Same as R408		
	R470	Same as R439		
	R471	Same as R440		
	R472	Same as R406		
	R473	Same as R432		
	R474	Same as R403		
	R475, 476	Same as R440		
	R477	Same as R408		
	R478	Same as R403		
	R479	Same as R446		
	R480	RESISTOR, fixed, composition, 47K, ±5%, 1/4 W	--	Ohmite
	R481	Not used		
	R482	Same as R428		
	R483	Same as R416		

Table 5-7. Parts List, Dropout Detector Board

FIG. NO.	REF. DESIG.	DESCRIPTION	PART NO.	MFR.
5-6		DROPOUT DETECTOR BOARD 45-400A --		HLI
	C1	CAPACITOR, film, 0.068 μF, 5%, 100 V dc	MW-R	Standard
	C2	CAPACITOR, film, 0.039 μF, 5%, 100 V dc	MW-R	Standard
	C3	CAPACITOR, film, 7500 pF, 5%, 100 V dc	MW-R	Standard
	C4, C5	CAPACITOR, film, 0.039 μF, 5%, 100 V dc	MW-R	Standard
	C6	CAPACITOR, tantalum, 1.0 μF, 10%, 35 V dc	CS13B	
	C7	CAPACITOR, electrolytic, 50 μF, 35 V dc	TAD	IEC
	C8	CAPACITOR, ceramic disk, 0.1 μF, 20 V dc	UK-20-104	Centralab
	C9	CAPACITOR, tantalum, 22 μF, 10%, 15 V dc	CS13B	
	C10	CAPACITOR, ceramic disk, 0.1 μF, 20 V dc	UK-20-104	Centralab
	C11	CAPACITOR, tantalum 22 μF, 10%, 15 V dc	CS13B	
	D1 thru D5	DIODE, silicon	1N3064	TI
	IC1 thru IC3	INTEGRATED CIRCUIT, dual operational amplifier	MC1458V	Motorola
	Q1	TRANSISTOR, silicon	2N5138	Fairchild
	R1	RESISTOR, fixed, composition, 10K, ±1%, 1/8 W	RN55D	Allen-Bradley
	R2	RESISTOR, fixed, composition, 20K, ±1%, 1/8 W	RN55D	Allen-Bradley
	R3 thru R5	RESISTOR, fixed, composition, 10K, ±1%, 1/8 W	RN55D	Allen-Bradley
	R6	RESISTOR, fixed, composition, 32.4K, ±1%, 1/8 W	RN55D	Allen-Bradley
	R7, R8	RESISTOR, fixed, composition, 20.5K, ±1%, 1/8 W	RN55D	Allen-Bradley
	R9	RESISTOR, fixed, composition, 12.1K, ±1%, 1/8 W	RN55D	Allen-Bradley

Table 5-7. Parts List, Dropout Detector Board (Cont)

FIG. NO.	REF. DESIG.	DESCRIPTION	PART NO.	MFR.
5-6	R10	RESISTOR, fixed, composition, 41.2K, ±1%, 1/8 W	RN55D	Allen-Bradley
	R11	RESISTOR, fixed, composition, 10.5K, ±1%, 1/8 W	RN55D	Allen-Bradley
	R12	RESISTOR, fixed, composition, 4.02K, ±1%, 1/8 W	RN55D	Allen-Bradley
	R13, R14	RESISTOR, fixed, composition, 10K, ±1%, 1/8 W	RN55D	Allen-Bradley
	R15	RESISTOR, fixed, composition, 2.2K, ±5%, 1/4 W	RCR07	Allen-Bradley
	R16	RESISTOR, fixed, composition, 1K, ±1%, 1/8 W	RN55D	Allen-Bradley
	R17	RESISTOR, variable, 1K, ±10%	72 PMR	Helipot
	R18	RESISTOR, fixed, composition, 2.2 megohm, ±5%, 1/4 W	RCR07	Allen-Bradley
	R19	RESISTOR, fixed, composition, 4.7K, ±5%, 1/4 W	RCR07	Allen-Bradley
	R20	RESISTOR, fixed, composition, 13K, ±1%, 1/8 W	RN55D	Allen-Bradley
	R21	RESISTOR, fixed, composition, 100 ohm, ±1%, 1/8 W	RN55D	Allen-Bradley
	R22	RESISTOR, fixed, composition, 100K, ±1%, 1/8 W	RN55D	Allen-Bradley
	R23, R24	RESISTOR, fixed, composition, 10K, ±1%, 1/8 W	RN55D	Allen-Bradley
	R25	RESISTOR, fixed, composition, 47K, ±5%, 1/4 W	RCR07	Allen-Bradley
	R26	RESISTOR, fixed, composition, 10K, ±5%, 1/4 W	RCR07	Allen-Bradley
	R27	RESISTOR, fixed, composition, 2.2K, ±5%, 1/4 W	RCR07	Allen-Bradley
	R28	RESISTOR, fixed, composition, 4.7K, ±5%, 1/4 W	RCR07	Allen-Bradley

Table 5-8. Parts List, Power Supply

FIG. NO.	REF. DESIG.	DESCRIPTION	PART NO.	MFR.
5-8	C301, 302	CAPACITOR, electrolytic, 250 μF, 25 V dc	45-101	HLI
	C303, 304	CAPACITOR, ceramic, 180 pF, 600 V dc	JK 180	RMC
	C305, 306	CAPACITOR, electrolytic, 100 μF, 25 V dc	45-102	HLI
	D301 thru D304	DIODE, silicon, 1N4001	--	Motorola
	D305	DIODE, silicon, 1N4148	--	Sylvania
	D306	DIODE, zener, 1N751 A	--	Int. Rect.
	D307 thru D310	Same as D305		
	D311, 312	Same as D301		
	Q301	TRANSISTOR, silicon, 38588	--	RCA
	Q302	TRANSISTOR, silicon, 39618	--	RCA
	Q303	TRANSISTOR, silicon, 2N4248	--	Fairchild
	Q304 thru Q307	TRANSISTOR, silicon, 2N3565	--	Fairchild
	Q308	Same as Q303		
	R301	RESISTOR, fixed, composition, 3.3 ohm, ±5%, 1/4 W	--	Allen-Bradley
	R302	RESISTOR, fixed, composition, selected, ±5%, 1/4 W	--	Ohmite
	R303	RESISTOR, fixed, composition, 1K, ±5%, 1/4 W	--	Ohmite
	R304	RESISTOR, fixed, composition, 2.2K ±5%, 1/4 W	--	Ohmite
	R305	RESISTOR, fixed, composition, 15K, ±5%, 1/4 W	--	Ohmite
	R306	RESISTOR, fixed, composition, 1.2K, ±5%, 1/4 W	--	Ohmite
	R307	RESISTOR, fixed, composition, selected, ±5%, 1/4 W	--	Ohmite
	R308, 309	RESISTOR, fixed, composition, 680 ohm, ±5%, 1/4 W	--	Ohmite
	R310	RESISTOR, fixed, composition, selected, ±5%, 1/4 W	--	Ohmite

Table 5-8. Parts List, Power Supply (Cont)

FIG. NO.	REF. DESIG.	DESCRIPTION	PART NO.	MFR.
5-8	R311	Same as R301		
	R312	Same as R302		
	R313	Same as R303		
	R314	Same as R304		
	R315	RESISTOR, fixed, composition, 10K, ±5%, 1/4 W	--	Ohmite
	R316	RESISTOR, fixed, composition, selected, ±5%, 1/4 W	--	Ohmite
	R317	RESISTOR, fixed, composition, selected, ±5%, 1/4 W	--	Ohmite
	R318	RESISTOR, fixed, composition, 4.7K, ±5%, 1/4 W	--	Ohmite
	R319	RESISTOR, fixed, composition, 5.1K, ±5%, 1/4 W	--	Ohmite
	T301	TRANSFORMER, power	45-103	HLI

Table 5-9. Parts List, Time Out Board

FIG. NO.	REF. DESIG.	DESCRIPTION	PART NO.	MFR.
5-10		TIME OUT BOARD HLI TO-1	--	
	C501, 502	CAPACITOR, paper, 0.22 μF, 75 V dc	225PZ	Sprague
	C503, 504	CAPACITOR, ceramic, 0.001 μF, 600 V dc	5GA	Sprague
	C506, 507	CAPACITOR, ceramic, 47 pF, 600 V dc	5GA	Sprague
	C508, 509	Same as C501		
	D501 thru D504	DIODE, silicon, 1N3064	--	Fairchild
	IC-501	INTEGRATED CIRCUIT, dual amplifier	MC 1437L or TOA 2809	Motorola Transitron
	Q501	TRANSISTOR, silicon, 2N5138	--	Fairchild
	Q502	TRANSISTOR, silicon, 2N3566	--	Fairchild
	R501, 502	RESISTOR, fixed, composition, 22K, ±5%, 1/4 W	--	Ohmite
	R503, 504	RESISTOR, fixed, composition, 10K, ±5%, 1/4 W	--	Ohmite
	R505	RESISTOR, fixed, composition, 100 ohm, ±5%, 1/4 W	--	Ohmite
	R506	RESISTOR, fixed, composition, 100K, ±5%, 1/4 W	--	Ohmite
	R507, 508	Same as R501		
	R509, 510	Same as R503		
	R511	Same as R505		
	R512	Same as R506		
	R513	Same as R501		

Table 5-10. Parts List, Frequency Translator Board

FIG. NO.	REF DESIG.	DESCRIPTION	PART NO.	MFR.
5-12		FREQUENCY TRANSLATOR BOARD	HLI GI-3	HLI
	C601 thru C606	CAPACITOR, trimmer, ceramic, 5-18 pF NPO	538-011A	Erie
	C607 thru C611	CAPACITOR, ceramic disc, 10 pF, 100 V dc, 10%	DD-100	Centralab
	C612	CAPACITOR, ceramic disc, 18 pF, 100 V dc, 10%	DD-180	Centralab
	C613 thru C618	CAPACITOR, ceramic disc, 0.1 μF, 10 V dc	UK-10-104	Centralab
	C619, 620	CAPACITOR, ceramic disc, 4700 pF, 1000 V dc, 20%	DD-472	Centralab
	C621	CAPACITOR, ceramic disc, 1000 pF, 1000 V dc, 10%	DD-102	Centralab
	C622	CAPACITOR, ceramic disc, 0.1 μF, 25 V dc	UK-25-104	Centralab
	C623 thru C625	CAPACITOR, tantalum, 2.2 μF, 25 V dc, 20%	--	Sprague
	C626	Not used		
	C627	CAPACITOR, mica, 390 pF, 600 V dc, 5%	CD7FA391	CDE
	C628	Same as C613		
	CR601	CRYSTAL, quartz, 437.000 kHz, 20 pF, load	CS	International Crystal
	CR602	CRYSTAL, quartz, 430.000 kHz, 20 pF, load	CS	International Crystal
	CR603	Not used (select option)		
	CR604	Not used (select option)		
	CR605	Not used (select option)		
	CR606	CRYSTAL, quartz, 454.000 kHz, 32 pF, load	CS	International Crystal
	F601	FILTER, ceramic, 455 kHz	TCF6-4D10A	Vernitron
	IC601, 602	INTEGRATED CIRCUIT, mixer-oscillator	MC 1357P	Motorola
	Q601	TRANSISTOR, silicon	2N3566	Fairchild
	R601	RESISTOR, fixed, 150 ohm, ±5%, 1/4 W	CB	Allen-Bradley

Table 5-10. Parts List, Frequency Translator Board (Cont)

FIG. NO.	REF DESIG.	DESCRIPTION	PART NO.	MFR.
5-12	R602, 603	RESISTOR, fixed, 2.4K, ±5%, 1/4 W	--	
	R604	Same as R601		
	R605, 606	RESISTOR, fixed, 220 ohm, ±5%, 1/4 W	--	
	R607	RESISTOR, fixed, 3.3K, ±5%, 1/4 W	--	
	R608	RESISTOR, fixed, 1.2K, ±5%, 1/4 W	--	
	R609, 610	RESISTOR, fixed, 620 ohm, ±5%, 1/4 W	--	
	R611	RESISTOR, fixed, 100 ohm, ±5%, 1/4 W	--	
	R612	Same as R607		
	R613	RESISTOR, variable, 20K, ±10%, 1/4 W	72PMR20K	Helitrim
	T601	TRANSFORMER	LF100100C	Vari-L

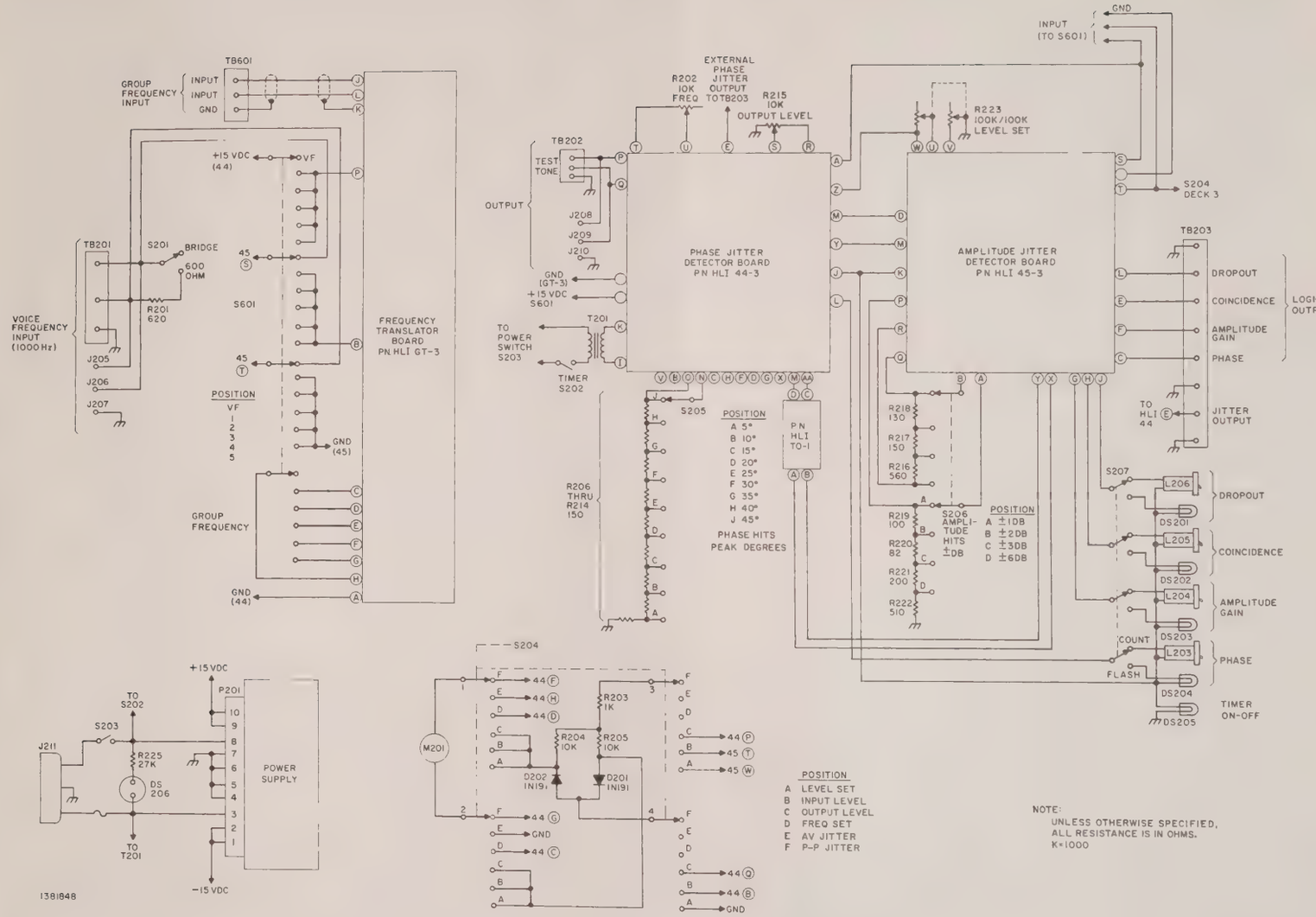
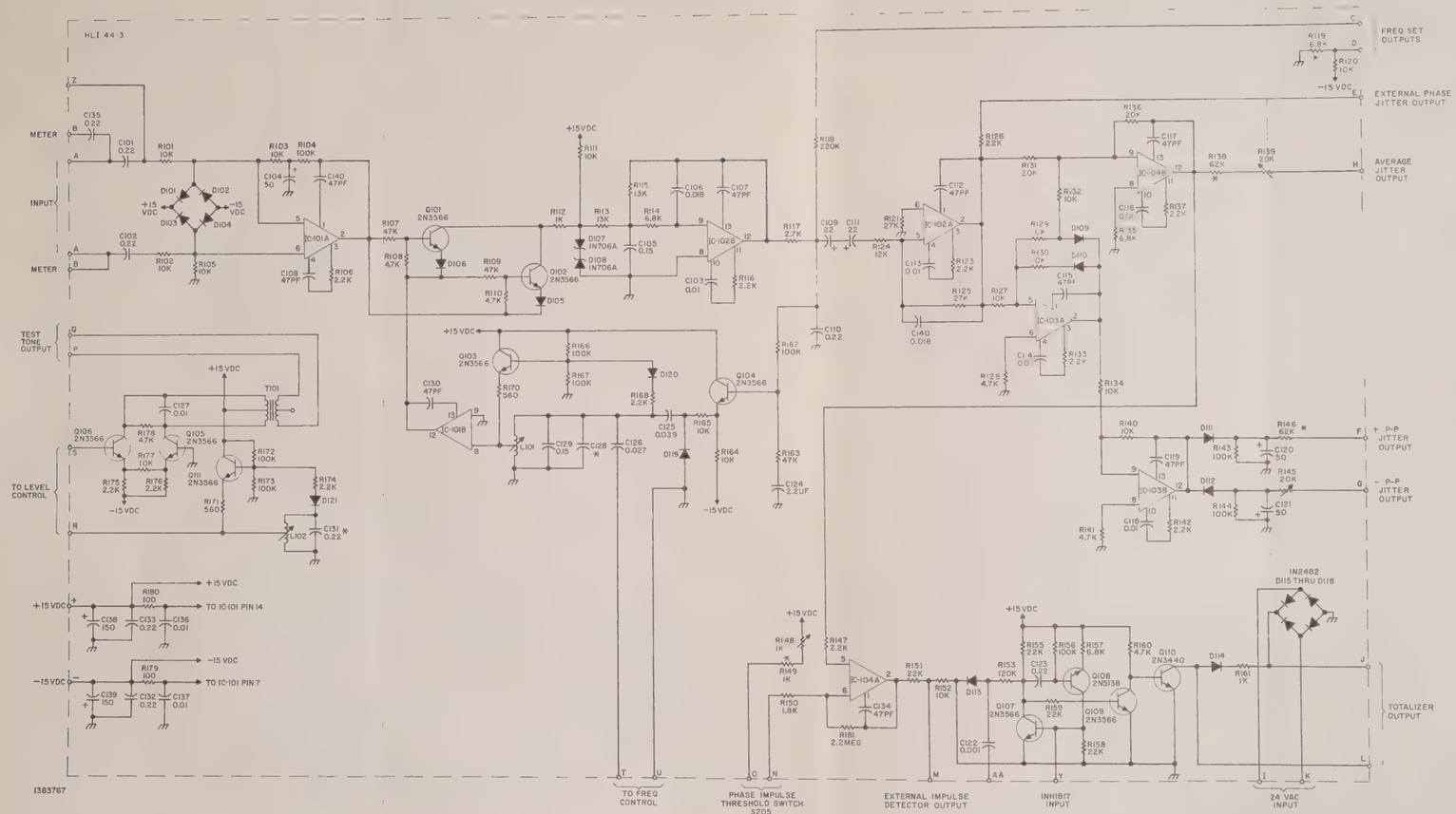


Figure 5-2. Model 45, Wiring Diagram



PIN DIAGRAMS
(BOTTOM VIEW)

NOTES:
1. +15 VDC APPLIED TO PIN NUMBER 14 ON IC-101 THRU IC-104
2. −15 VDC APPLIED TO PIN NUMBER 7 ON IC-101 THRU IC-104
3. ALL UNSPECIFIED DIODES, IN3064
4. IN THE MODEL 45 THE FOLLOWING COMPONENTS ARE DELETED
   C 101, 102
   D 101, 102, 103, 104
   R 102, 151, 152
   R 151 IS REPLACED WITH A JUMPER
5. C138, 139 ARE USED ONLY IN THE MODEL 45.

* SELECTED VALUE NORMAL VALUE SHOWN

Figure 5-3. Phase Jitter Detector Board, Schematic Diagram

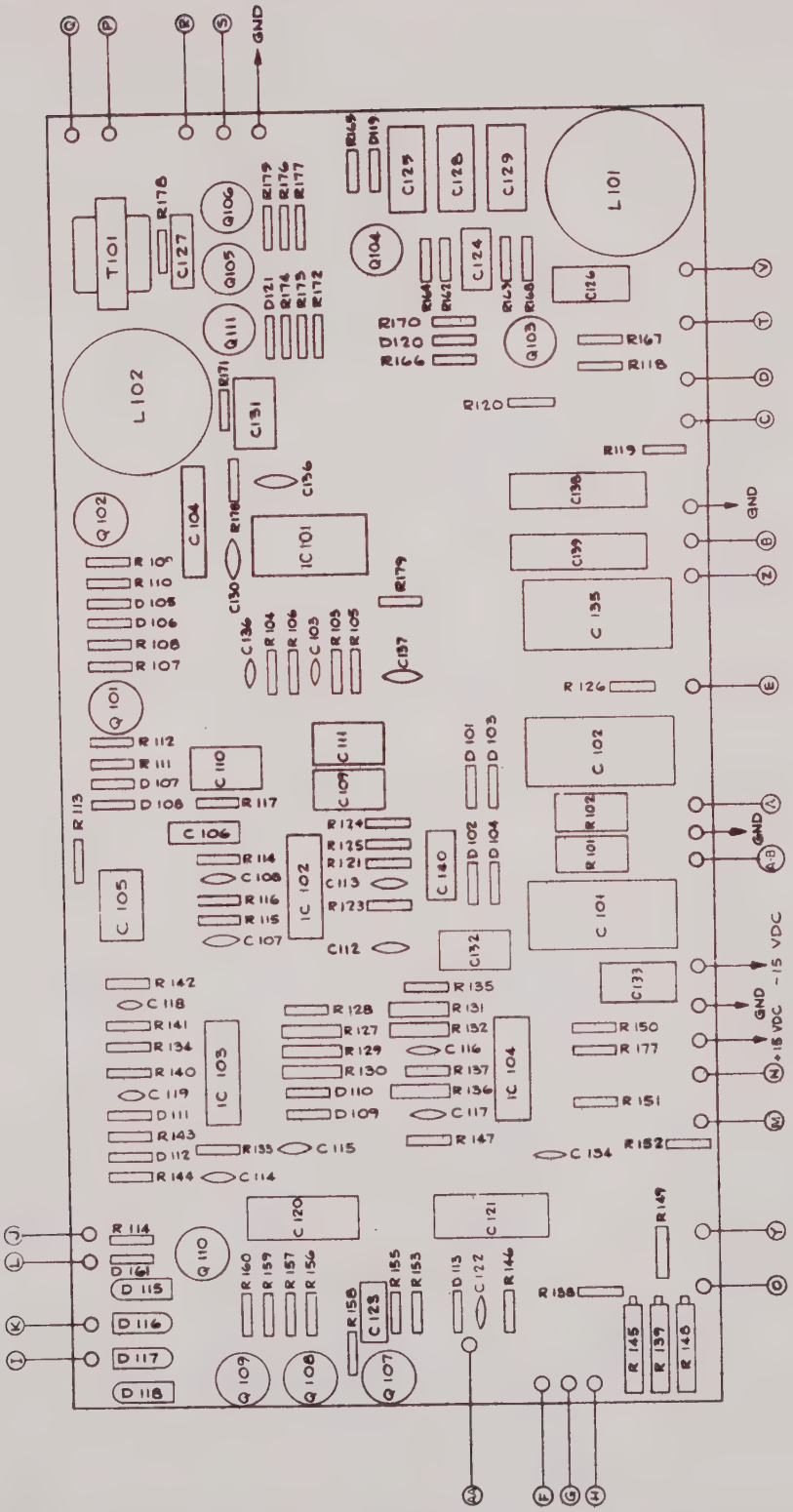


Figure 5-4. Phase Jitter Detector Board, Component Layout

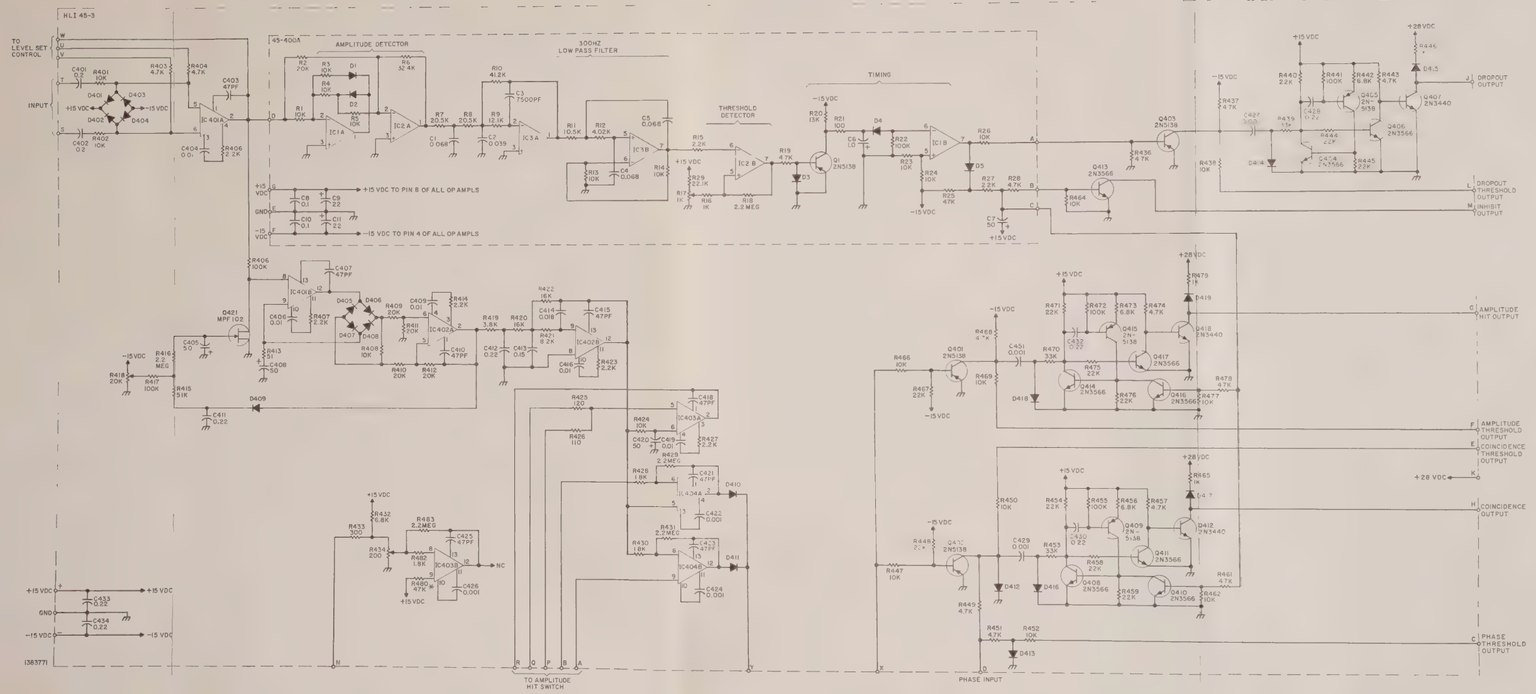
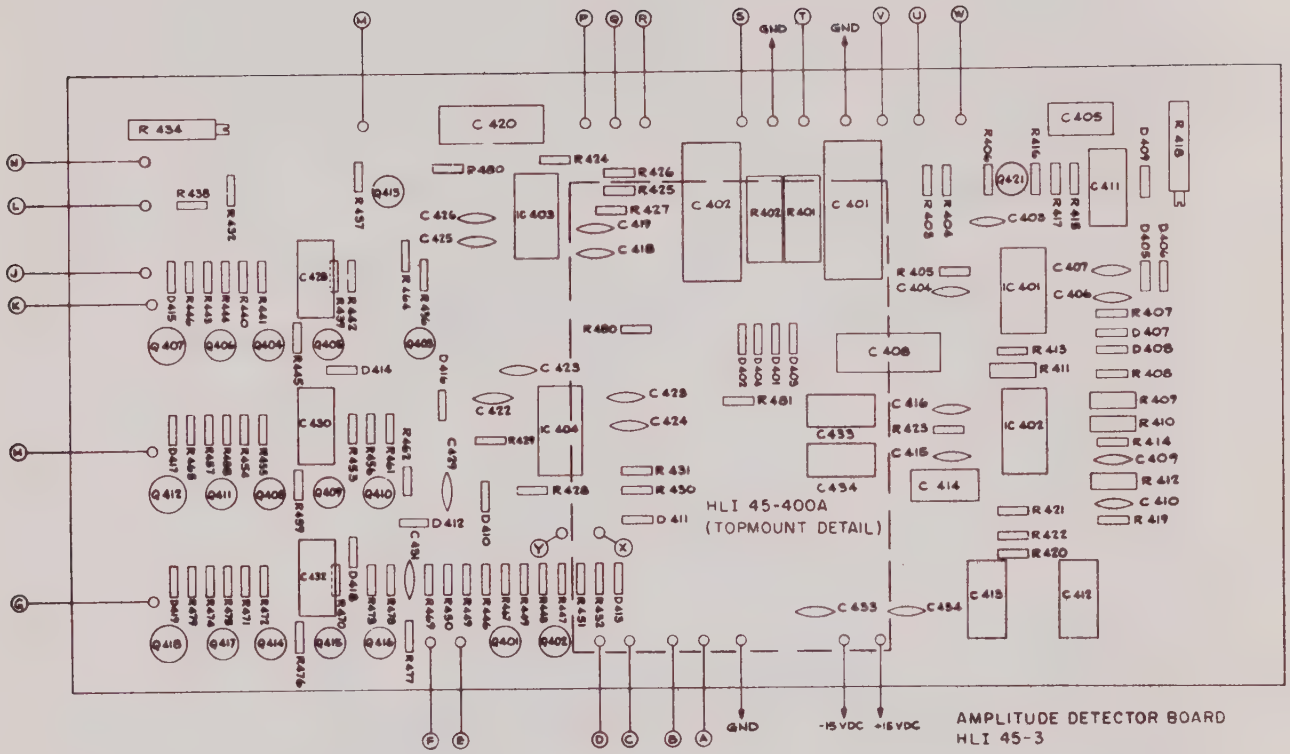
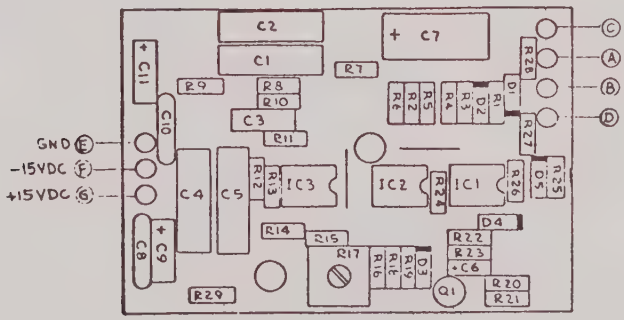


Figure 5-5. Amplitude Detector Board, Schematic Diagram





DROPOUT DETECTOR BOARD
HLI 45-400A
(TOPMOUNT DETAIL)

Figure 5-6. Amplitude Detector Board, Component Layout

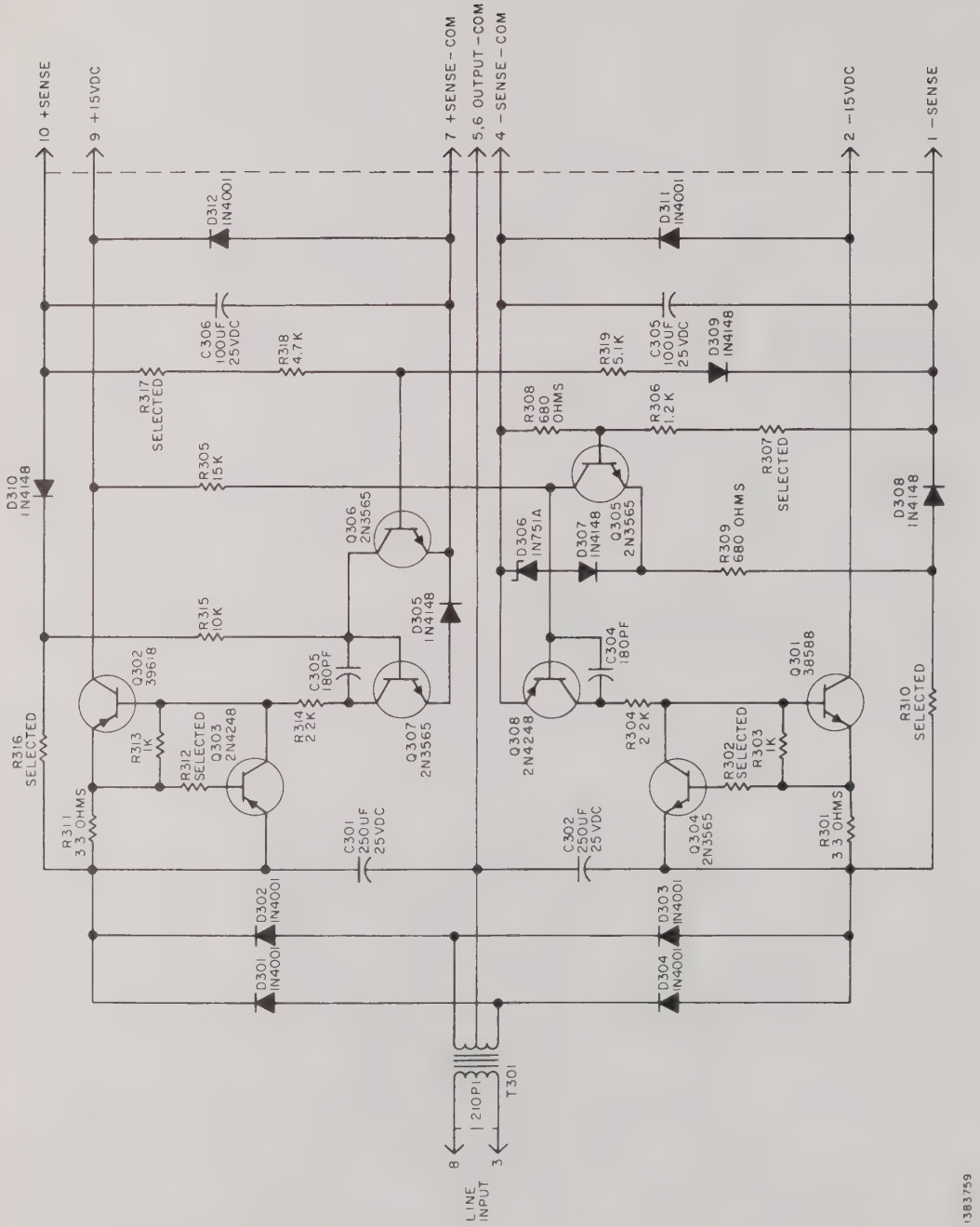


Figure 5-7. Power Supply, Schematic Diagram

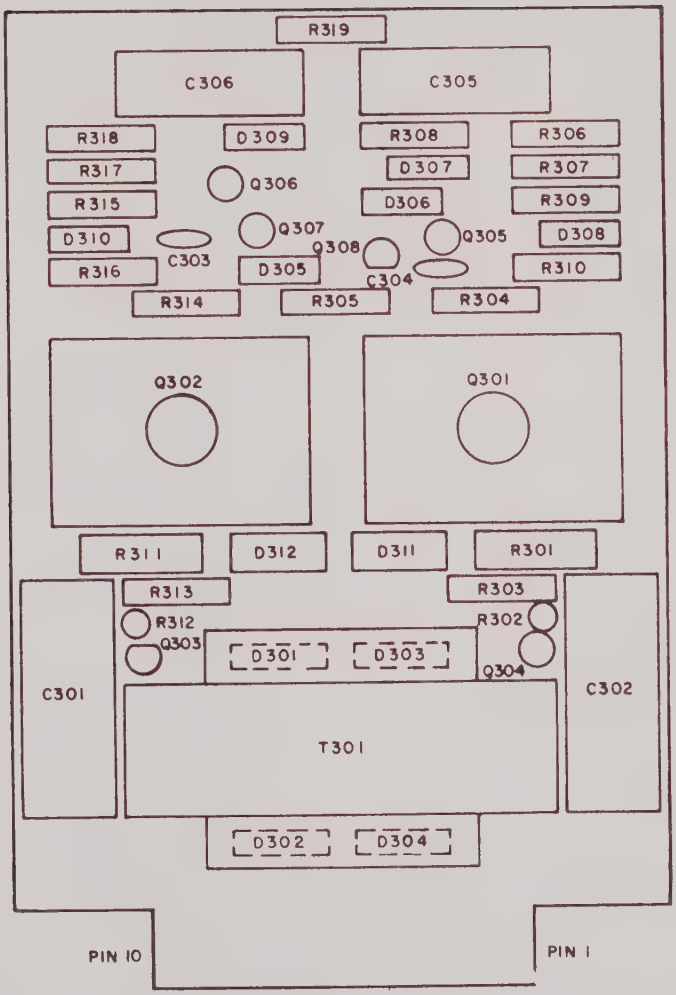


Figure 5-8. Power Supply Board, Component Layout

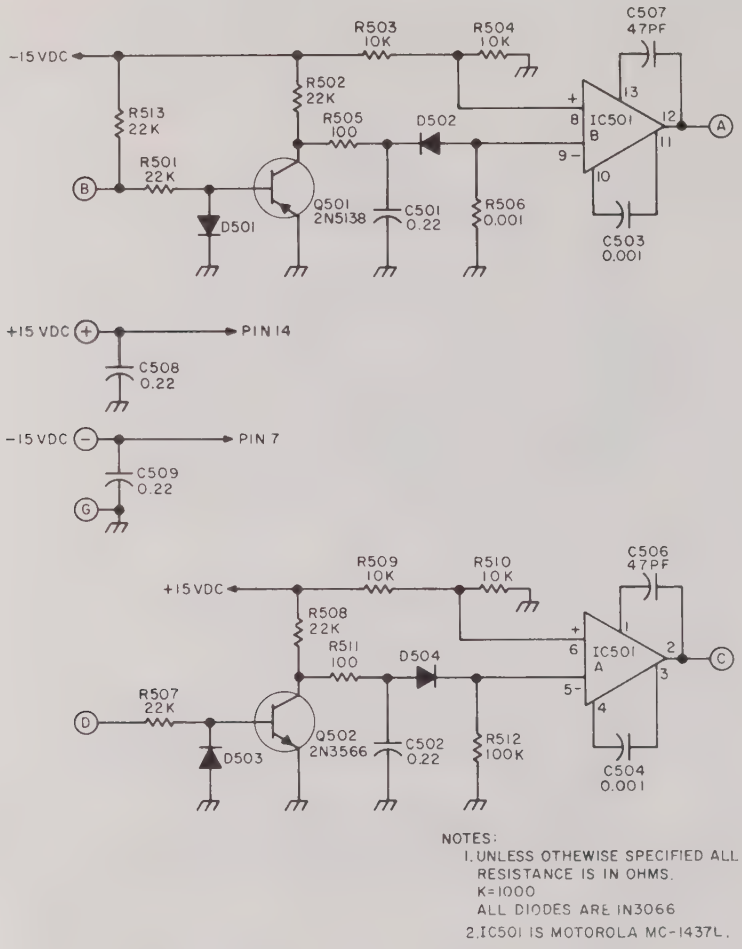


Figure 5-9. Time Out Board, Schematic Diagram

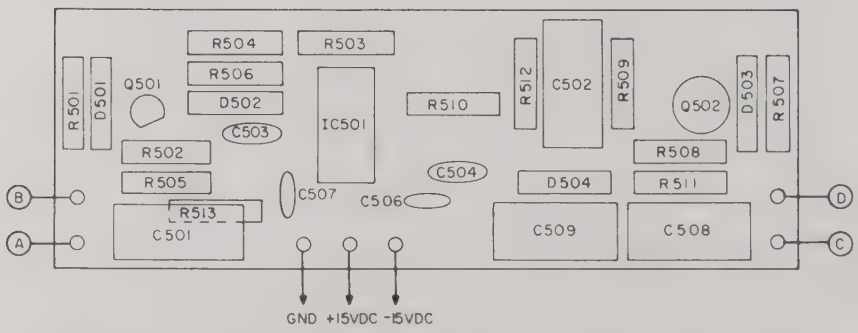


Figure 5-10. Time Out Board, Component Layout

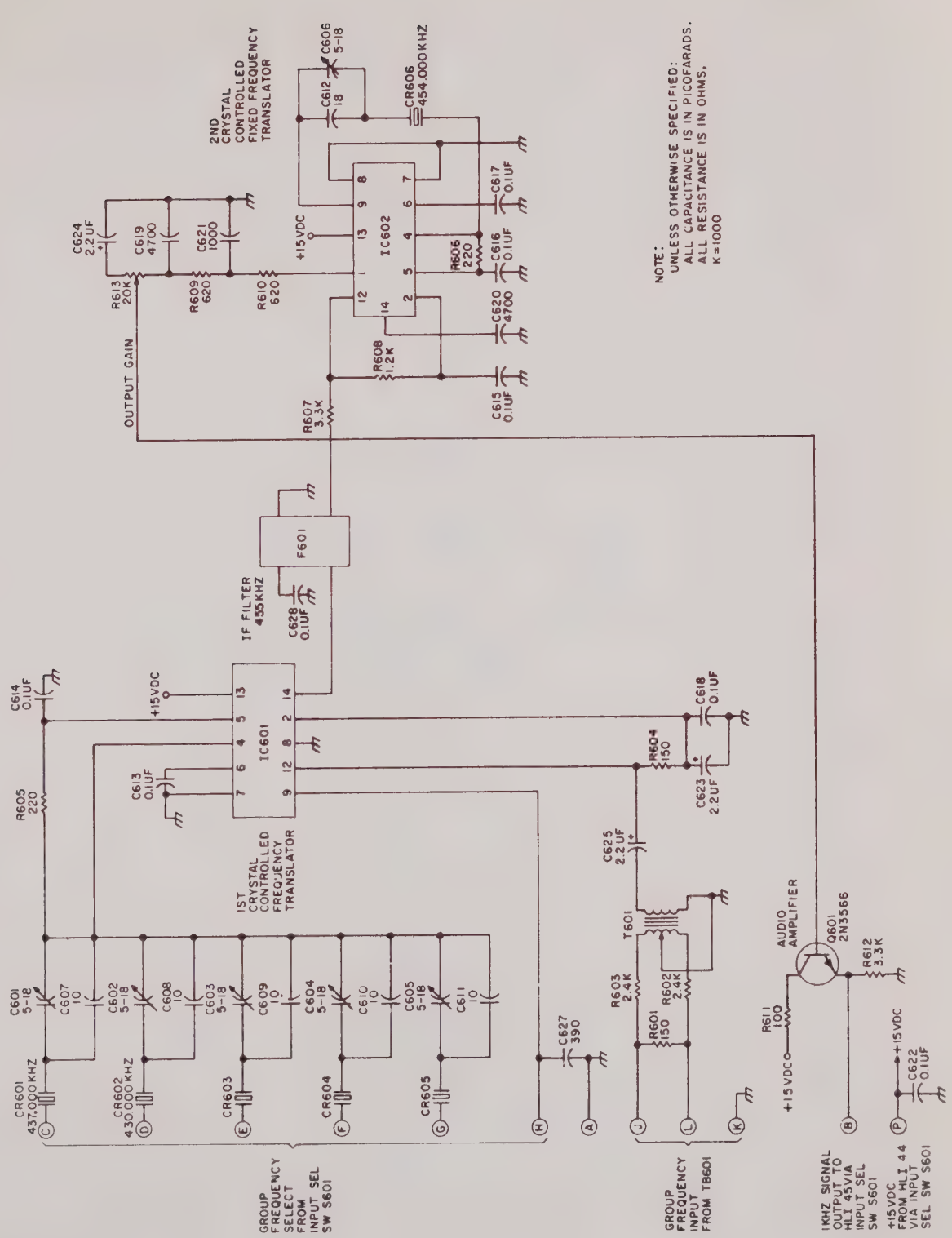


Figure 5-11. Frequency Translator Board, Schematic Diagram

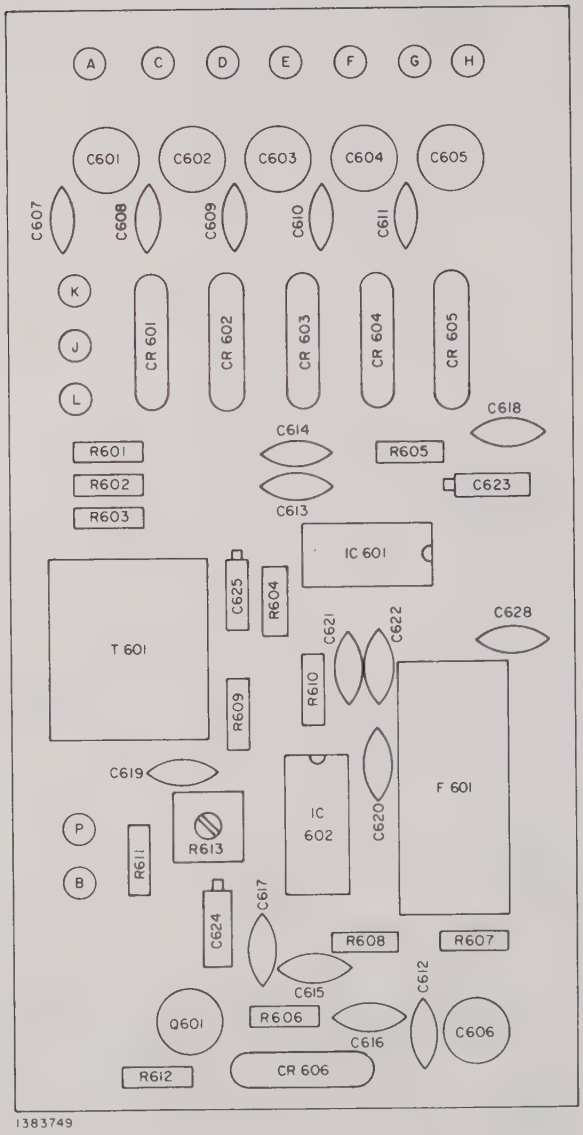


Figure 5-12. Frequency Translator Board, Component Layout

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